SUBCONTRACT TITLE: ***ADVANCED PROCESSING OF CdTe- AND $CuIn_{1-X}Ga_XSe_2$- BASED SOLAR CELLS***

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Part I – CdTe

EXECUTIVE SUMMARY

This project addresses two thin film technologies CdTe and CIGS. The CdTe component of the project has three task areas. These are:

- development and evaluation of novel front and back contacts
- development of simplified processing for the fabrication of CdTe solar cells
- correlation of the long term stability with process/device characteristics

Successfully addressing these areas will lead to the fabrication of efficient and stable CdTe solar cells and modules.

During the first year of this project stability studies focused on the effect of the $CdCl_2$ treatment on cell stability. CdTe devices were heat treated at various temperatures and subsequently light soaked for a period of 1000 hours. The cells where kept in an inert ambient and were held at short and open-circuit conditions. The need for a large number of data in order to eliminate one-of-a-kind type of behavior makes this type of activity labor intensive. To address this issue a system has been designed and is currently under construction that will automatically test – collect J-V data - for a large number of samples.

In the area of front contacts emphasis has been placed on ternary transparent conductors and buffer layers. Materials under consideration include Cd_2SnO_4, Zn_2SnO_4, and $CdIn_2O_4$. Devices are fabricated using bi-layer structures where the top layer is a high resistivity or a "buffer" layer. The films are deposited using co-sputtering of either the constituent binary oxides or metals in oxygen ambient.

The focus on back contacts remains on the "Cu-free" type. However, it appears that the lack of Cu limits considerably the performance of CdTe cells. To-date the most successful "Cu-free" back contact option remains the one previously developed and based on Ni_2P. Efforts during this phase of the project to directly deposit Ni_2P on CdTe are yet to produce any promising results. In this report the most recent Sb_2Te_3 efforts are also summarized, as this approach will no longer be pursued.

Work on simplifying the overall cell fabrication process is also underway. The two subtasks in this area include a vapor $CdCl_2$ heat treatment and a large area high-throughput CSS-type deposition system for the deposition of CdTe and CdS. The results from the vapor treatment are very encouraging, and suggest that the typical wet $CdCl_2$ process can be replaced without sacrificing performance. The large area CdTe deposition system has been brought on-line, with initial work being focused on uniformity issues, with regards to films and device performance.

All devices are routinely characterized using in-house analytical techniques, and whenever necessary additional analysis is carried out in collaboration with other Thin Film Partnership participants and NREL. The University of South Florida continues to participate in the CdTe National Team activities in various ways including processing samples from other laboratories/companies or supplying samples for analysis/stress etc.

1.0 INTRODUCTION

The main tasks of this project address the critical issues of the CdTe technology. These are performance, manufacturability, and long term stability. The activities focus on specific processes and device components. For example in the area of manufacturability emphasis is placed on eliminating wet processing steps such as the $CdCl_2$ heat treatment, as well as studies associated with the close-spaced sublimation process where a new deposition system capable of coating 10 x 10 cm^2 moving substrates has been brought on line. More details on the specific tasks will be provided in the next section where the cell fabrication procedures are outlined. Cell analysis is based on basic solar cell measurements such as dark and light current-voltage (J-V), monochromatic J-V, spectral response (SR), and capacitance-voltage (C-V) measurements. Whenever appropriate, additional analysis is carried out in collaboration with NREL or other CdTe Thin Film Partnership members.

2.0 CELL FABRICATION PROCEDURES

Although additional details and variations of the CdTe cell fabrication procedures can be found elsewhere, most of the key processes are described here along with the tasks addressed during the first year of the project [1].

All cells discussed in the report are of the typical CdTe superstrate configuration:

Glass/TCO layer(s)/window/CdTe/back contact.

Wherever the term "baseline device" is used it applies to cells fabricated with the following configuration and deposition procedures:

Corning 7059 glass/SnO_2:F/SnO_2/CBD-CdS/CSS-CdTe/doped graphite.

(a) ***Glass substrates***: Two types of glass substrates are being utilized. Borosilicate glass (Corning 7059) is the baseline substrate and is used routinely in all processes/structures. Soda lime glass, typically LOF TEC 15, is also used when cells are processed at low temperatures (<550ºC).

(b) ***Front Contact***: The baseline transparent conducting oxide (TCO), is tin oxide (SnO_2) prepared by CVD and doped with fluorine. The TCO is typically a bi-layer structure where a "high resistivity" or a "buffer" layer is deposited on top of the conductive one[†]. Currently a series of ternary TCO's based on Cd, Zn, Sn, and In are under consideration. These are deposited using (co-) sputtering of the binary oxides, or reactive sputtering of metallic targets.

(c) ***Window Layer:*** Cadmium sulfide (CdS) is the primary window layer, although frequently this layer is left out of the solar cell structure, to determine whether some of the TCO's under investigation can be used as effective replacements. Cadmium sulfide is prepared by two techniques, chemical bath deposition (CBD) and close spaced sublimation (CSS). The CSS is favored as a manufacturing friendly process, however, cell performance is consistently higher when CBD CdS films are used, and therefore this process is being used for the fabrication of baseline devices.

(d) ***Cadmium Telluride***: Thin films of CdTe are being deposited by the CSS process. Currently, all devices are fabricated using small area (deposition area approx. 3 x 3 cm^2) CSS depositions systems. During the first year of this project a larger area semi-automated system, with substrate motion has been brought on-line and is being optimized for uniformity and performance.

[†] The term "buffer" will be used in this report to describe high resistivity transparent oxides; such films were incorporated in bi-layer (high/low resistivity) front contact structures.

(e) ***$CdCl_2$ Heat Treatment:*** This process has been one of the key activities in efforts to simplify the overall cell fabrication process by eliminating all wet processing steps. In addition to direct application of the $CdCl_2$ to the CdTe surface prior to heat treatment, a vapor treatment has also been implemented and is under development. During the initial phase of this project, work using a small area annealing apparatus (3 x 3 cm^2 sample size) has continued, but a large area vapor treatment system (four 3 x 3 cm^2 substrates) has been constructed in order to investigate spatial non-uniformities noted while utilizing the small area unit. The substrate temperature and ambient during the $CdCl_2$ heat treatment have been the primary process parameters studied during this phase.

(f) ***Back Contact:*** Doped graphite is the primary method of back contact formation. Small amounts of dopants (in powder form) such as HgTe:Cu, Cu, or Ni_2P are mixed with graphite paste and subsequently applied onto the CdTe surface. Alternatively, sputtered options are also being utilized and these include Cu_XTe, Ni_2P, and Sb_2Te_3. Although in the past a cleaning/etching step of the CdTe surface in a bromine/methanol solution has been used prior to back contact formation, during this project in an effort to eliminate wet processes this step is being omitted for some samples treated with vapors of $CdCl_2$.

3.0 ALTERNATIVE WINDOW LAYERS – TRANSPARENT CONDUCTING OXIDES

Work on alternative window layers and transparent conducting oxides/buffer layers has over the last two years focused on studies involving binary and ternary oxides based on Cd, Sn, In, and Zn. While SnO_2 and ITO have been widely used in CdTe applications, other materials with better electro-optical properties such as Cd_2SnO_4 have been utilized to further enhance the performance of CdTe cells [2]. In addition to improving conductivity and transmission, the use of bi-layer transparent contacts (low resistivity/high resistivity) has also been proven beneficial to solar cell performance. Finally, CdS continues to be the best suited heterojunction partner for CdTe thin film solar cells but its band gap combined with the difficulty of depositing continuous thin (<1000Å) films leads to current losses of several mA/cm^2. Although, replacing the CdS has not yet produced the desired results, combining thin CdS with the appropriate transparent "buffer" has lead to the fabrication of record cells [2].

The first group of TCO/buffer layers studied includes Cd_2SnO_4, $CdIn_2O_4$, and In_2O_3. Sputtered SnO_2 is also being used as a buffer layer (baseline SnO_2 films are prepared by CVD). In the case of ternary compounds, since these films are deposited by co-sputtering, it is possible to vary their stoichiometry. One of the first issues addressed in each case was the effect of the metal ratio on the electro-optical and structural properties of the films. After initial optimization of the films' properties these were incorporated into solar cell structures. The following sections describe to-date results as they relate to the first year of this project.

3.1 Deposition Conditions

As already mentioned above the deposition process for alternative TCO's/buffers is sputtering. Table 1 provides a summary of the range of deposition conditions used for the films being investigated. Two 3" magnetron rf sputtering sources were mounted approximately 10 cm away from a rotating substrate holder; the angle between the sputtering source and a normal to the substrate holder was about 23º. The deposition area was approximately 8 x 8 cm^2. The power density used for each source did not exceed 4.2 W/cm^2; the power level depended on the type of material and desired deposition rate. The uniformity of the deposited films over the entire deposition area has been studied and found to be within 1-2% over the entire deposition area. Larger variations exist at the edges of the samples where shadowing effects from the sample holder affect the deposition.

Table 1. Summary of Deposition Conditions for the Sputtered TCO's

Film	Target Material(s)		Ambient	Pressure [mTorr]	Substrate Temp. [ºC]
Cd_2SnO_4	CdO (4N)	SnO_2 (4N)	Ar	3-4	RT
$CdIn_2O_4$	Cd (4N)	In (5N)	Ar/O_2(25%)	1-3	RT
Zn_2SnO_4	ZnO (5N)	SnO_2 (4N)	Ar	3-4	RT to 450
In_2O_3	In (5N)	----	Ar/O_2(25%)	3-4	RT to 400

3.2 Cadmium Stannate (Cd_2SnO_4)

3.2.1 Resistivity

A previous report included information on the effect of the Cd to Sn ratio on resistivity, and the effect of annealing temperature on crystallinity and film composition [1]. The effect of annealing on the resistivity of Cd_2SnO_4 is displayed in Fig. 1, where the ratio of the as-deposited over the annealed resistivity is shown. The films were deposited using the "optimum" Cd to Sn ratio as established from previous work (a Cd/Sn ratio of approximately 2.1 resulted in the lowest resistivity), and subsequently annealed in inert ambient (He). The temperature range was chosen in order to include the lowest temperature at which the films were found to begin to crystallize (i.e. 550ºC); no temperatures higher than 700ºC were used due to the limitations of the glass substrates, but also due to the fact that such temperatures are not practical for solar cell processing. Film resistivity improves in all cases (i.e. all annealed films exhibit lower resistivity than the as-deposited ones), by up to one order of magnitude. However, as the annealing temperature increases the resistivity decreases less. At high annealing temperatures (700ºC) the Cd_2SnO_4 films were found to decompose (the SnO_2 phase was detected in such films), which is believed to be part of the reason for the observed increased resistivity. Another reason is the change in grain size, which was found to decrease as the annealing temperature was increased[†].

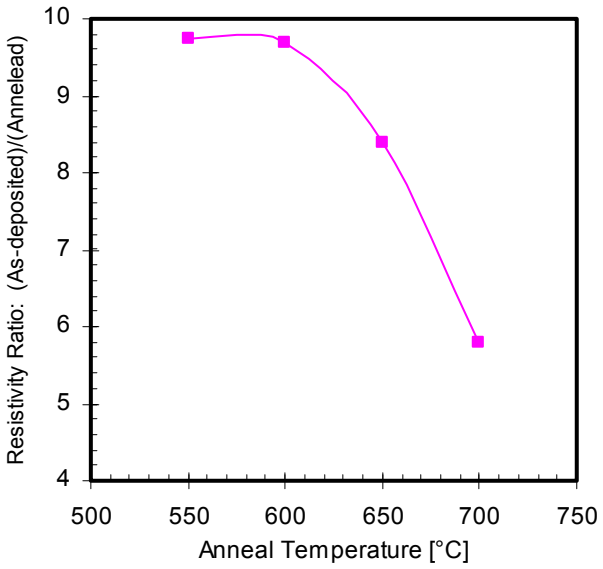


Figure 1. The ratio of as-deposited to annealed resistivity of Cd_2SnO_4 films

3.2.2 Surface Properties

It has been previously reported that one of the advantages of Cd_2SnO_4 compared to SnO_2 is its relative smoothness [3]. In the case of CdTe solar cells, a smoother TCO can facilitate the deposition of thin and continuous CdS films. Figure 2 shows AFM images of a Cd_2SnO_4 before and after annealing at 600ºC in He[‡]. This film was deposited to a thickness of 3000 Å at room

[†] The grain size was calculated using Sherer's equation.
[‡] Note that although the two image areas are equal (1 µm square), the vertical axes are 20 and 50 nm for the as-deposited and annealed films respectively.

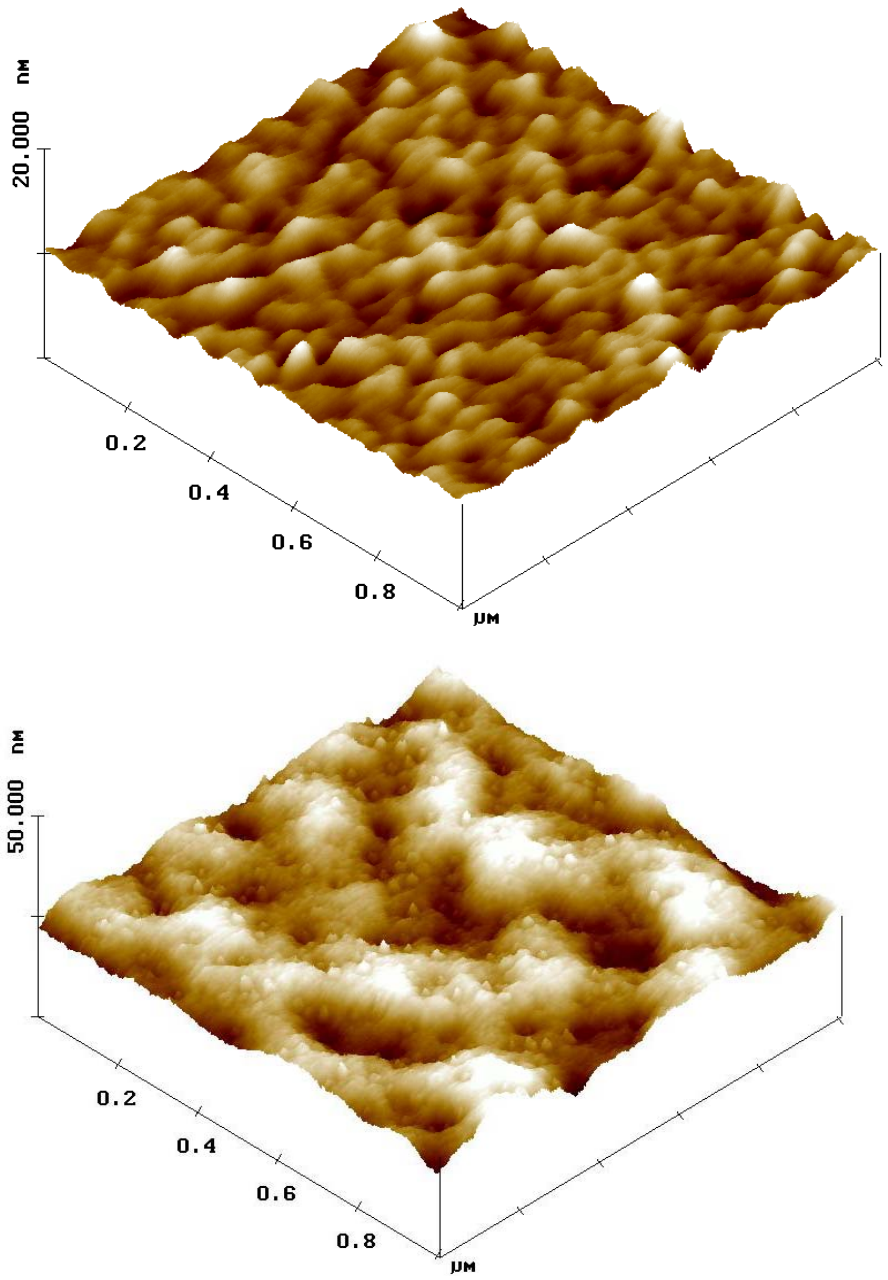


Figure 2. AFM images of as-deposited (top) and annealed @ 600ºC (bottom) Cd_2SnO_4 films

temperature, and using metal ratio conditions for minimum resistivity [1]. The surface roughness for the as-deposited film, which was amorphous, was approximately 0.40 nm. The annealed film exhibited a roughness of 1.40 nm, which is at the low end of previously reported values of 1.3 to 3.2 [4,5]. It is not clear what the origin of small features visible in the image of the annealed film is. It is possible that these are the beginning of a secondary phase formation, however, this could not be confirmed using XRD measurements, which revealed a SnO_2 phase only in films annealed at 700ºC.

3.3 Cadmium Indium Oxide ($CdIn_2O_4$)

Most work on $CdIn_2O_4$ was carried under a different program and the influence of the Cd to In ratio on the electro-optical and structural properties of these films has been reported[6]. Further analysis of the surface of the $CdIn_2O_4$ films was carried out during this project prior to incorporating these in solar cell structures.

Figure 3 shows AFM images for $CdIn_2O_4$ films annealed at 300, 400, 500, and 600ºC in He ambient. These films were prepared using conditions that were previously found to yield the lowest resistivity[6]. The images of Fig. 3 appear to be consistent with the crystal structure and composition as determined with XRD analysis. The films were found to begin to crystallize between 300 and 400ºC, with higher annealing temperatures, up to 500ºC, leading to further improvement in crystallinity; at 600ºC the films were found to contain the In_2O_3 phase[6]. The 400 and 500ºC images of Fig. 3 clearly show the onset of crystallization and grain growth. The rather "abraded" appearance of the 600ºC image is believed to be a result of $CdIn_2O_4$ decomposition as suggested by the presence of the In_2O_3 phase in such films. Film roughness ranged from approximately 2.3 to 3.5 nm for single phase $CdIn_2O_4$ films, which is higher than what was obtained for Cd_2SnO_4.

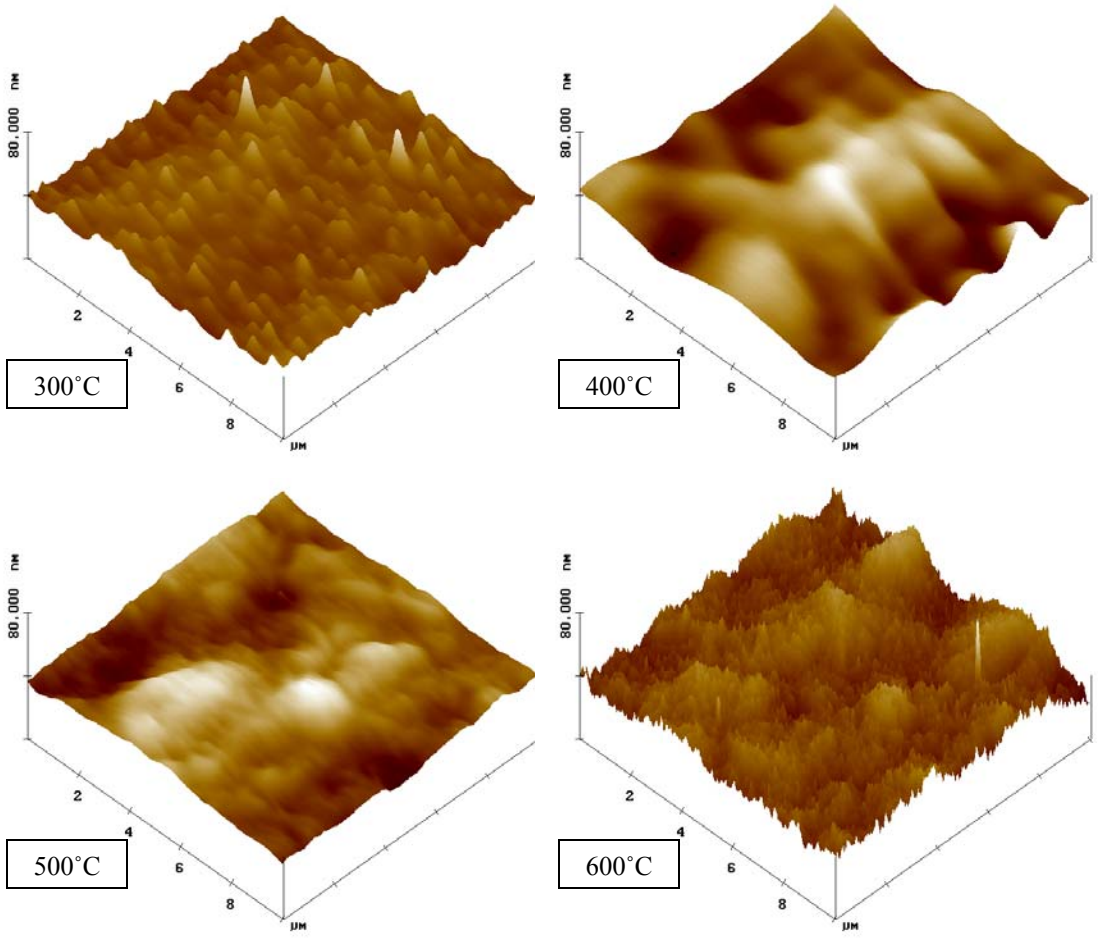


Figure 3. AFM surface images of 10 µm^2 sections of $CdIn_2O_4$ films annealed at different temperatures in He

3.4 Resistive Transparent Films (Buffers)

This section describes work carried out on "buffer" layers. The inclusion of a resistive layer between the CdS and the conductive TCO has been found to be beneficial to device performance. Although, the exact mechanism is not very well established yet, it is believed that such a layer prevents the CdTe from coming in direct contact with the conductive TCO, especially at regions where the CdS is very thin. This prevents the formation of localized CdTe/TCO junctions which are inferior to CdTe/CdS and tend to degrade the overall cell performance. The most recent example is based on zinc stannate (Zn_2SnO_4) which has been utilized for the fabrication of record efficiency CdTe cells[7,8]. Sputtered In_2O_3 and SnO_2 as well as Zn_2SnO_4 (a capability developed under a different program) are being investigated. Although CVD SnO_2 served as the baseline material, sputtered SnO_2 is being considered due to the manufacturing advantages of the sputtering process.

3.4.1 Indium Oxide (In_2O_3)

As indicated in table 1, In_2O_3 was prepared by reactive sputtering using a metallic target in an Ar/O_2(25%) ambient. While, in the case of ternaries such as Cd_2SnO_4 a significant portion of the effort focused on post-deposition annealing due to the fact that as-deposited films were found to be amorphous regardless of the temperature of deposition[†], in the case of In_2O_3 higher substrate temperatures produced polycrystalline films. Figure 4 shows the XRD patterns obtained for In_2O_3 films deposited at temperatures up to 400ºC. It is clear that for deposition temperatures up to 200ºC the films are amorphous (patterns for RT and 100ºC films are not shown as they were identical to the 200ºC films). The films deposited at the two highest temperatures, exhibit preferential orientation along the (222) direction, with the 400ºC film

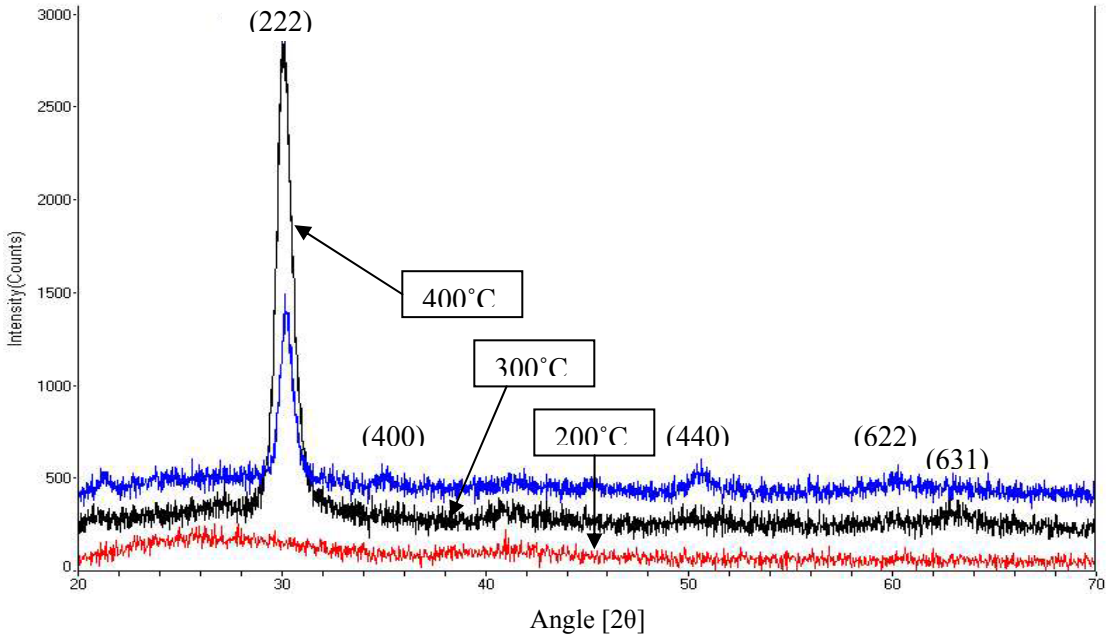


Figure 4. X-ray diffraction patterns for reactively sputtered In_2O_3 deposited at different temperatures

[†] Maximum deposition temperatures attainable using the existing deposition system cannot exceed 450ºC.

displaying a stronger signal indicative of improved crystallinity.

The four point probe resistivity and sheet resistance of 2000Å thick In_2O_3 films as a function of the deposition temperature is shown on Fig. 5. As indicated the resistivity decreases with deposition temperature. Nevertheless it is high (as expected) making the films suitable as buffer layers but not as transparent contacts. Films deposited at lower temperatures exhibited too high resistivity and were not measurable with the same method.

The optical transmission of In_2O_3 films was found to be high (on average over 90%) and was nearly identical for amorphous and polycrystalline films.

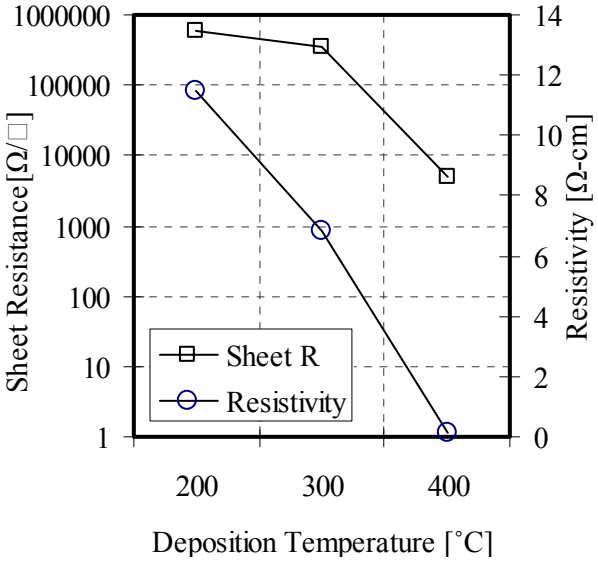


Figure 5. Sheet resistance and resistivity as a function of deposition temperature for reactive sputtered In_2O_3 films

3.4.2 Tin Oxide (SnO_2) by Sputtering

Baseline CdTe solar cells fabricated at USF utilize a bi-layer SnO_2 front contact prepared by CVD. Such devices have exceeded cell efficiencies of 15.0%. During this project sputtered SnO_2 has been used as a buffer layer. Films have been prepared by both reactive sputtering from a Sn target, and conventional sputtering from a SnO_2 target.

3.4.2.1 SnO_2 from a SnO_2 Target

Tin oxide films prepared from a SnO_2 target were deposited in an Ar/O_2(25%) ambient, as films deposited without O_2 did not exhibit the required optical properties. They had a brown color presumably due to a high concentration of oxygen vacancies. It should be noted that the target itself had a similar color i.e. the starting material was O_2 deficient.

The crystallographic properties of this type of SnO_2 exhibited a strong dependence on the substrate temperature as indicated in Fig. 6. Room temperature films are not included in this figure as they exhibited a similar featureless pattern as the films deposited at 100ºC. The films begin to crystallize at temperatures between 100 to 200ºC with essentially random orientation. At 300ºC the films are preferentially oriented along the (110) direction, but as the temperature is further increased to 400ºC the intensities of the (101) and (211) peaks increase relative to the (110) and the films appear to become randomly oriented. Along with the change toward a random orientation, a secondary phase was also detected for the film deposited at 400ºC. A peak not associated with SnO_2 appeared at a slightly larger 2θ than the (200) peak. This was not identified as SnO_2 based on the PDF file used (file number 71-0652); although not confirmed, this peak is believed to me associated with tin monoxide (SnO).

The resistivity for the same set of SnO_2 films is shown in Fig. 7. The amorphous films (deposited at the lowest substrate temperatures) exhibit the highest resistivity as expected. All

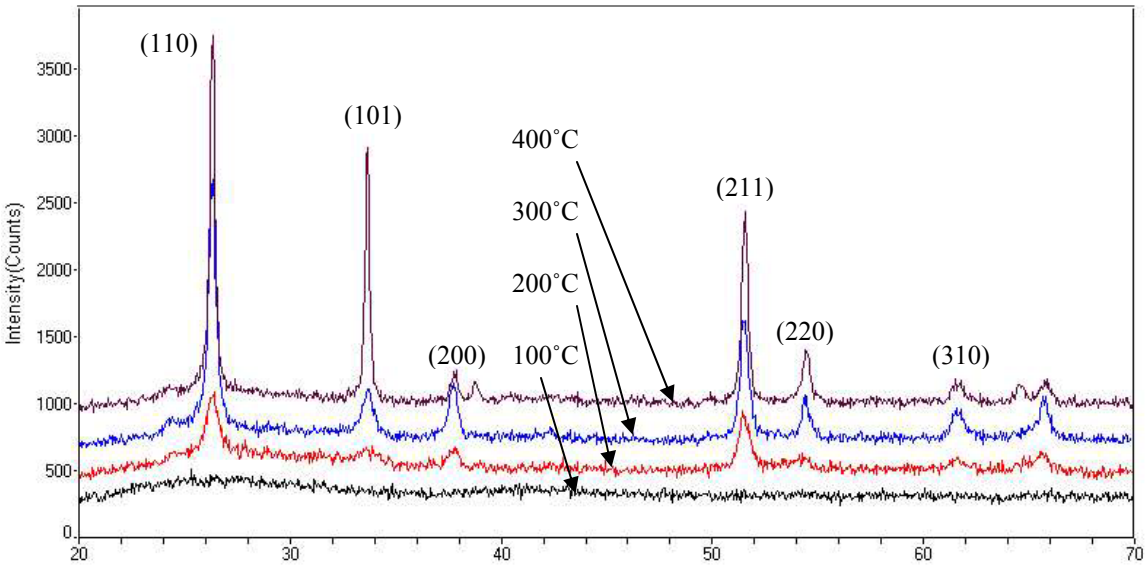


Figure 6. X-ray diffraction patterns for SnO_2 (from a SnO_2 target) sputtered at different substrate temperatures

polycrystalline films have significantly lower resistivities than the amorphous ones, with the film deposited at 200ºC, having the lowest resistivity of all. It is possible that the observed change in orientation and possibly grain size for the films deposited at 300 and 400ºC is responsible for the modest increase in these films' resistivity.

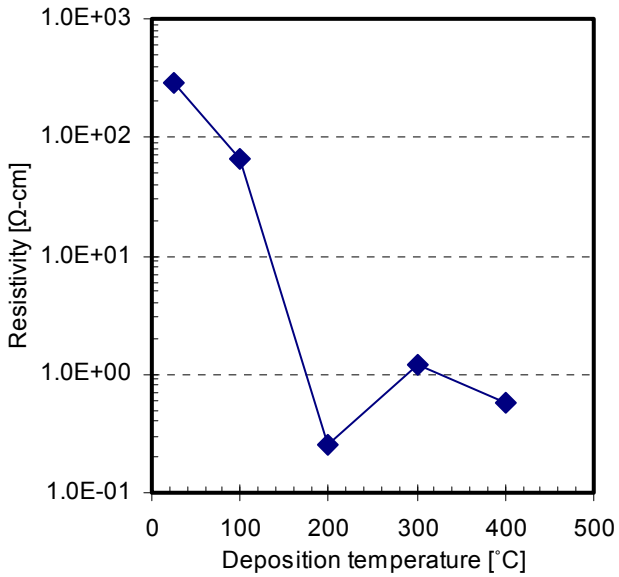


Figure 7. The resistivity of SnO_2 films shown in Fig. 6

3.4.2.2 SnO_2 by Reactive Sputtering

Based on structural information obtained for films sputtered from a SnO_2 target, a number of SnO_2 films were prepared at 300ºC using reactive sputtering. It was initially assumed that the two approaches would essentially yield films with very similar properties; however, with regards to structural properties that was not the case. Figure 8 displays XRD data for a reactively sputtered film from a SnO_2 target. As the data suggests these films exhibit a higher degree of preferential orientation along the (110) direction, compared to the SnO_2 films of Fig. 6. The lower signal intensity for the film shown in Fig. 8 (compared with films in Fig. 6) is partly due to the smaller thickness of this film. Therefore, it appears that the process dynamics are significantly different between the two approaches. At this time no further analysis has been carried out on reactively sputtered films, other than utilizing them in solar cells (to be discussed in a subsequent section).

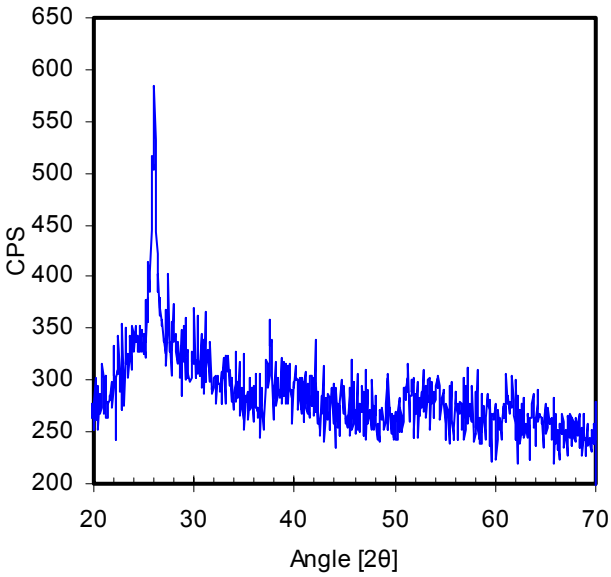


Figure 8. XRD pattern for a reactively sputtered SnO_2 film (T_{SUB}=300ºC)

3.5 Solar Cells

In this section, solar cell results based on combinations of the above discussed TCO's and buffers are presented.

3.5.1 $CdIn_2O_4$-based Solar Cells

3.5.1.1 Solar Cells without a Buffer Layer

Prior to fabricating cells based on a bi-layer TCO structure, a set of CdTe/CdS devices were fabricated directly onto $CdIn_2O_4$. The cells were fabricated on as-deposited (RT) and annealed at 300, 400, and 500ºC $CdIn_2O_4$ films. The effect of annealing on $CdIn_2O_4$ has been discussed elsewhere[6]; briefly, as-deposited films are amorphous and restive while heat treated films (T>400ºC) are polycrystalline with low resistivity (resulting in 10-20 Ω/□ sheet resistance).

Figure 9 shows the light J-V data for the $CdIn_2O_4$/CdS/CdTe devices. The cells fabricated on $CdIn_2O_4$ annealed at the two highest temperatures clearly exhibit improved performance primarily due to higher V_{OC}'s. The solar cell parameters for these devices are listed in table 2. The V_{OC} is at least 100 mV higher for the cells fabricated on $CdIn_2O_4$ annealed at the two highest temperatures. The FF is also higher for these cells by 3-7%; differences in J_{SC} are only 0.3 mA/cm^2, and based on the SR (see Fig. 10), they are primarily due to "deep" losses.

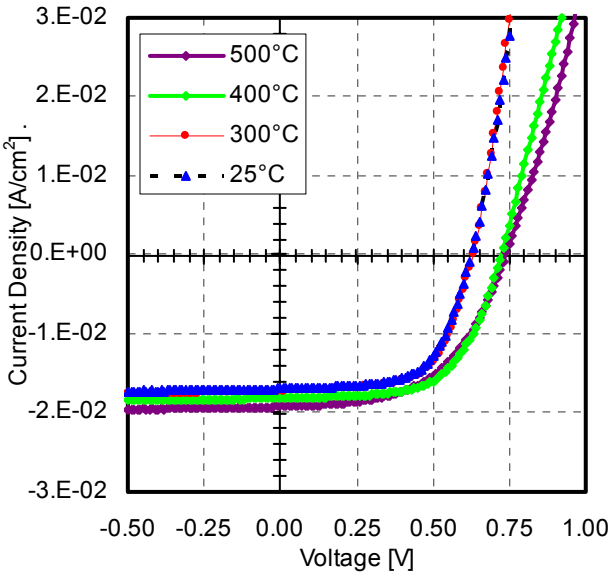


Figure 9. Light J-V data for $CdIn_2O_4$/CdS/CdTe solar cells

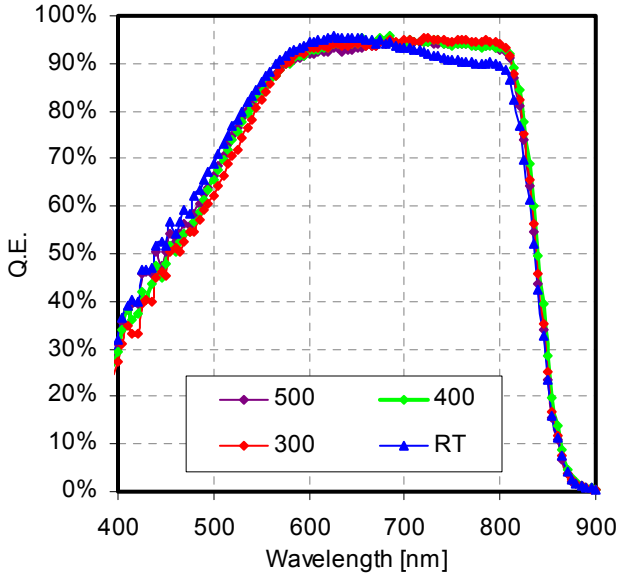


Figure 10. SR data for the cells displayed in Fig. 9

Table 2. $CdIn_2O_4$/CdS/CdTe Solar Cell Characteristics

Annealing Temperature [ºC]	V_{OC} [mV]	FF	J_{SC} [mA/cm^2]
500	760	0.62	23.5
400	755	0.61	23.6
300	645	0.58	23.3
As-deposited	619	0.54	23.3

Several possibilities exist that can explain the above results: (a) The nucleation of CdS onto the $CdIn_2O_4$ films can vary significantly since the structure of the substrate varies. This could impact the proprieties of the CdTe/CdS interface/junction. (b) As indicated above, the $CdIn_2O_4$ films annealed at 300ºC as well as the as-deposited ones are initially amorphous. Although their structure after the cell fabrication was completed is not known, it is believed that they were partially crystallized, due to the fact that they were exposed to high temperatures (near 600ºC) for times of approximately 4-6 minutes. It should also be noted that the resistivity of the as-deposited $CdIn_2O_4$ film improves significantly after the cells are completed (based on the series resistance of the finished device), which supports the above claim that the films must have partially crystallized. This "crystallization" of $CdIn_2O_4$ during the cell fabrication process could affect significantly the properties of the junction; even affect the properties of CdS, if traces of In from $CdIn_2O_4$ outdiffuse into the CdS.

Based on the slope of these cells in reverse bias it appears that the shunt resistance for all cells is similar indicating $CdIn_2O_4$ does not to cause any shunting regardless of its properties. The SR of the same devices is shown in Fig. 10. As previously mentioned the only significant difference lies in the 700-850 nm range. It seems that collection in the two devices, as-deposited and annealed at 300ºC, is inefficient in this region. This may be caused by either the strength/distribution of the collecting field or variations in the diffusion lengths in the various cells. Based on all these results it is clear that $CdIn_2O_4$ can have a significant effect on the junction properties of CdTe solar cells. Annealing at 500ºC improves the robustness of these films. It is notable that the performance of these devices i.e. without a "buffer" layer is better than a similar structure with SnO_2.

3.5.1.2 Solar Cells with Buffer Layers

In order to establish a baseline performance, the first buffer layer used with $CdIn_2O_4$ was CVD SnO_2. Table 3 lists the V_{OC} and FF for CdTe solar cells fabricated on $CdIn_2O_4$ with and w/o the CVD SnO_2 buffer layer. The gains in both V_{OC} and FF are obviously quite significant when a buffer layer is used.

Table 3. The Effect of CVD SnO_2 Buffer Layer on $CdIn_2O_4$-based Solar Cells

Substrate	V_{OC} [mV]	FF
$CdIn_2O_4$ (HT @ 500ºC)	760	0.62
$CdIn_2O_4$ (HT @ 500ºC)/CVD-SnO_2	837	0.71

Figure 11 displays the light J-V characteristics for cells fabricated on $CdIn_2O_4/In_2O_3$ substrates including the slope of each set i.e. (dV/dJ). For these devices, the In_2O_3 films were deposited at 300ºC while the $CdIn_2O_4$ films were deposited at room temperature and subsequently annealed at the same temperatures as the cells discussed in the previous section. Table 4 lists the solar cell characteristics of these devices including series resistance.

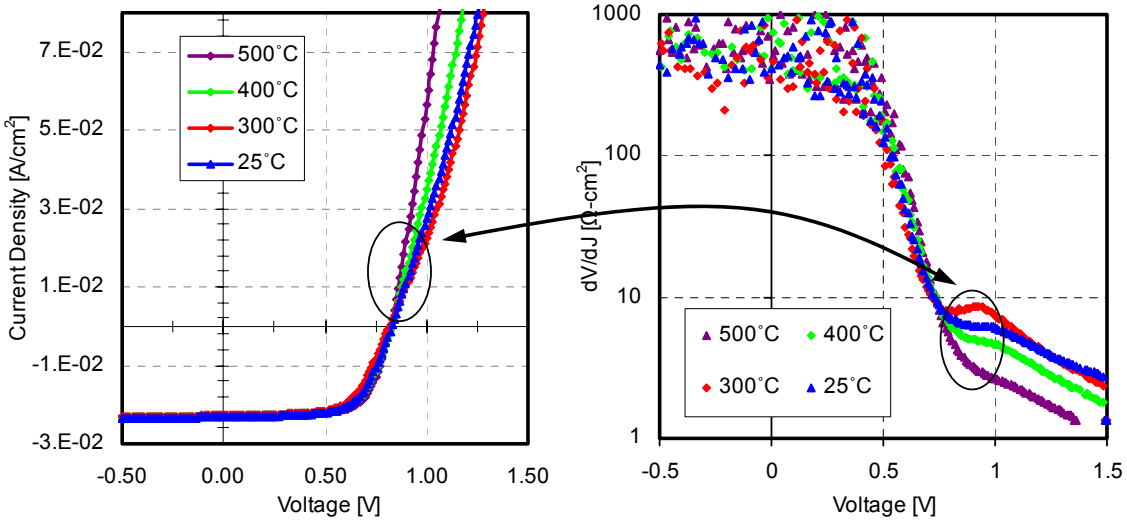


Figure 11. Left - Light J-V data for CdTe cells fabricated on $CdIn_2O_4/In_2O_3$ substrates; right – (dV/dJ) data for the same cells

Table 4. $CdIn_2O_4/In_2O_3$/CdS/CdTe Solar Cell Characteristics

Annealing Temperature [ºC]	V_{OC} [mV]	FF	J_{SC} [mA/cm^2]	R_{SERIES} [Ω-cm^2]
500	825	0.69	23.2	1.52
400	826	0.66	23.0	2.79
300	820	0.64	22.8	2.84
As-deposited	830	0.66	23.2	3.15

Compared to the cells fabricated without a buffer, these devices exhibit V_{OC}'s at least 70 mV higher. Unlike the cells listed in table 2, in this case the influence of the $CdIn_2O_4$ layer is minimized and the only significant effect appears to be an increase in series resistance that lowers the FF for devices with $CdIn_2O_4$ that was initially amorphous. This was expected since the as-deposited and annealed at 300ºC films were resistive prior to being processed into

complete devices, but as already discussed above their resistivity improved during the solar cell fabrication process. Nevertheless, based on the results listed in table 4, the series resistance for the cells prepared on the initially amorphous films is higher than cells prepared on films annealed at 400 and 500ºC (i.e. polycrystalline prior to cell fabrication). The slope (dV/dJ) of the J-V data is also included in Fig. 11. It is evident from this graph that only the device with $CdIn_2O_4$ annealed at 500ºC appears to have a relatively "well behaved" slope, one that does not display the effect of a back barrier. All others seem to suggest that the corresponding devices are affected by a barrier which is presumably responsible for a portion of the series resistance component measured (see marked regions in Fig. 11). The SR for the same cells is shown in Fig. 12. All cells exhibit essentially identical SR with small differences in the short wavelength range, a region greatly influenced by small variations in the CdS thickness. The long wavelength region where devices discussed in the previous section exhibited a dependence on the properties of $CdIn_2O_4$ appears to be identical. Therefore, In_2O_3 is an effective "buffer" layer, by "restoring" the V_{OC} and improving the FF of these cells; however, the effect of the conductive layer (in this case $CdIn_2O_4$), is not completely "eliminated" by the inclusion of a buffer, as it leads to the formation of what appears to be a barrier that affects the J-V characteristics of the cells at voltages slightly above V_{OC}, and causes an increase in the series resistance. When $CdIn_2O_4$ is heat treated at the optimum temperature, cell performance improves and the series resistance decreases considerably.

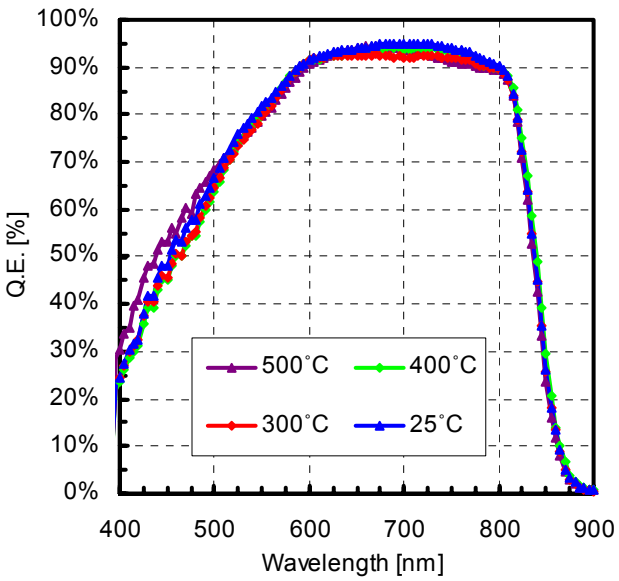


Figure 12. SR for the cells shown in Fig. 11

3.5.1.3 Collection in $CdIn_2O_4$-based Solar Cells

As discussed in the previous two sections, solar cells fabricated without a buffer layer were inferior to those with In_2O_3 or SnO_2 as buffer layers. In addition to inferior V_{OC}'s and FF's some of the cells fabricated without a buffer also suffered from what was identified in Fig. 10 as poor collection. To further address this issue the devices were characterized using monochromatic light. Four wavelengths were selected for this measurement, 460, 540, 640, and 800 nm. The longer the wavelength the deeper the light penetration and therefore the carrier generation will be. At each wavelength the light intensity was adjusted to correspond to the equivalent of AM1.5 within the 20 nm bandwidth of the interference filters. The monochromatic J-V data for a $CdIn_2O_4$-based cell fabricated without a buffer layer are shown in Fig. 13; a plot of the FF vs. wavelength for cells with and without buffer layers is shown in Fig. 14. The dotted lines represent the white light AM1.5 FF for each cell. In all cases the FF's are decreasing with wavelength indicating that collection for deep carriers is not efficient. The cell fabricated with the CVD SnO_2 buffer exhibits the highest FF at 460 nm; for the three longer wavelengths its FF is equal to that of the cell with In_2O_3 as a buffer. The FF of the cell without the buffer layer is high at 460 nm, but decreases to a greater extent than the other two devices for longer wavelengths. The above results suggest that the use of a buffer layer improves carrier collection by most likely affecting the distribution of the collecting field, or by influencing the

properties of CdTe leading to improved diffusion lengths. The use of In_2O_3 has produced results nearly identical to those achieved using CVD-SnO_2, suggesting that In_2O_3 is indeed an effective buffer. Nevertheless, in all cases the FF decreased with wavelength suggesting that all devices can be furthered improved by enhancing collection. It should be noted that the highest monochromatic FF (CVD-SnO_2 @ 460 nm) was approximately 77% while the white FF for the same device was only about 71%.

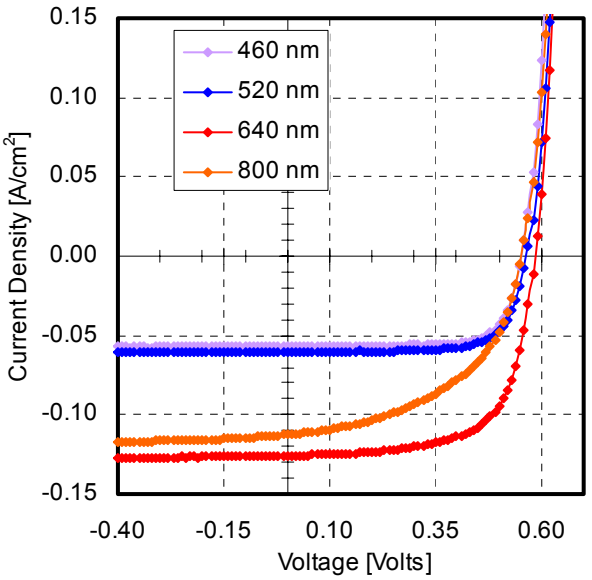


Figure 13. Monochromatic light J-V for a $CdIn_2O_4$-based cell w/o a buffer layer

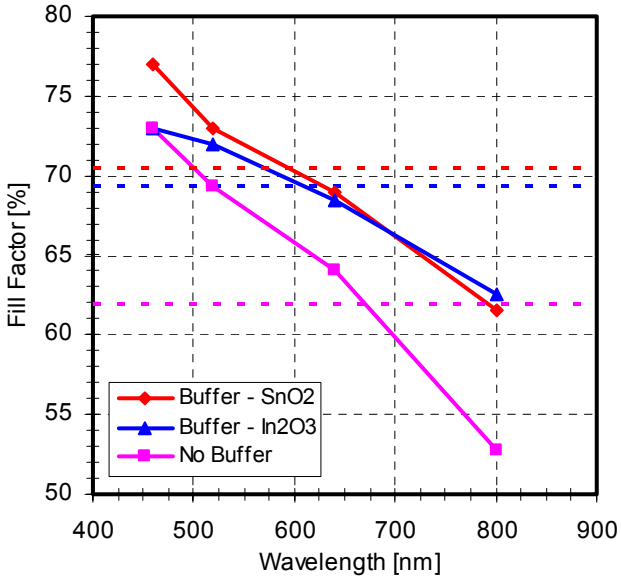


Figure 14. The dependence of the FF on wavelength for $CdIn_2O_4$-based solar cells

3.5.2 Cd_2SnO_4-based Solar Cells

Solar cell results from Cd_2SnO_4/CdS/CdTe solar cell results were presented in a previous report[1]. The solar cell parameters for these cells are included in table 5 below. As these results indicate the use of Cd_2SnO_4 even without a buffer can yield V_{OC}'s in excess of 800 mV and FF's approaching 70%.

Table 5. Solar Cell Performance for Cells Fabricated on Cd_2SnO_4 without a Buffer Layer

Cd_2SnO_4 thickness [Å]	V_{OC} [mV]	J_{SC} [mA]	FF [%]
1000	825	23.56	68.3
1500	808	23.48	67.3
2000	821	23.10	69.6

The subsequent sections summarize results from solar cells fabricated using Cd_2SnO_4 as the TCO and SnO_2 as a buffer. Tin oxide was deposited using three different processes: (a) by sputtering from a SnO_2 target, (b) by reactive sputtering from a Sn target, and (c) by CVD (baseline process).

3.5.2.1 SnO_2 by Sputtering of a SnO_2 Target

Resistivity and structural data as a function of the substrate temperature for SnO_2 films sputtered from a SnO_2 target have been provided in a previous section. As indicated films deposited at 300ºC were found to be the most highly oriented. Tin oxide was deposited onto Cd_2SnO_4 at three different deposition temperatures, 200, 300, and 400ºC. The Cd_2SnO_4/SnO_2 bi-layers were subsequently used for solar cell fabrication using standard procedures (i.e. CBD-CdS and CSS-CdTe). Light J-V characteristics for representative solar cells are shown in Fig. 15 and table 6 lists the solar cell parameters for the same devices.

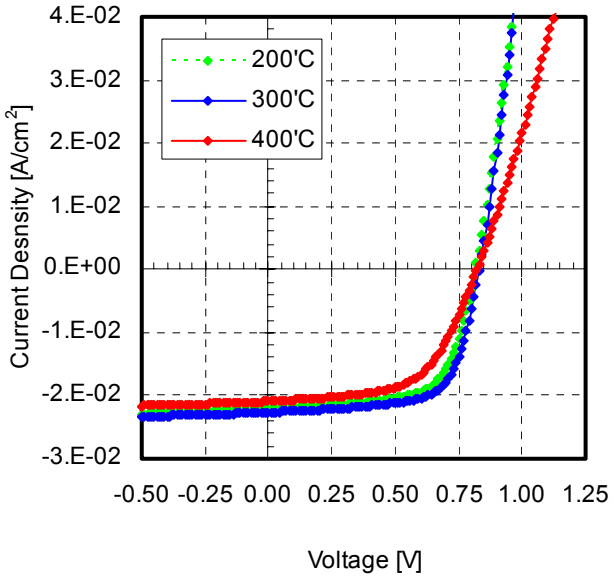


Figure 15. Light J-V characteristics of CdTe cells fabricated on Cd_2SnO_4/SnO_2 bi-layers

Table 6. Solar Cell Parameters for CdTe Cells Fabricated on Cd_2SnO_4/SnO_2(Reactive Sputtering) Substrates

SnO_2 Deposition Temperature [ºC]	V_{OC} [mV]	FF	J_{SC} [mA/cm^2]
200	815	0.66	22.9
300	830	0.68	23.1
400	822	0.58	23.2

The V_{OC} for all devices is above 810 mV with the device with SnO_2 deposited at 300ºC having the highest value of 830 mV. Short-circuit current values are very similar and only vary within a narrow range of 0.2-0.3 mA/cm^2. Based on the SR data shown in Fig. 16, there appear to be small variations in the short wavelength region (most likely due to variations in the CdS thickness), but also at longer wavelengths where the device fabricated with SnO_2 deposited at 200ºC exhibits the lowest response, suggesting that collection for deeply absorbed photons is poor in this cell. The other significant difference in the characteristics of these cells is obviously variations in their FF. The 400ºC SnO_2 cell appears to be dominated by a high series resistance, with the other two devices exhibiting subtle differences around V_{MAX}. It is not clear what caused the

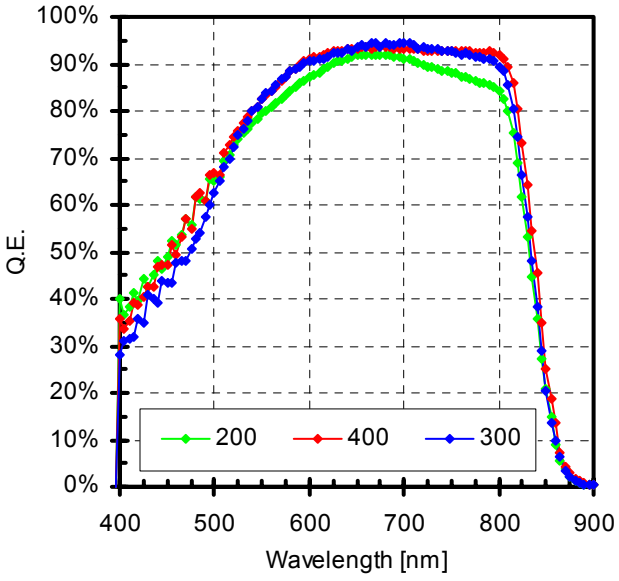


Figure 16. SR of cells shown in Fig. 15

high series resistance for the 400ºC device, since as indicated in a previous section SnO_2 films sputtered at 200, 300, and 400ºC all exhibited similar resistivity. It is possible that the resistivity of the SnO_2 deposited at 400ºC increased during the cell fabrication process; however, this is something that must be confirmed. Overall, cells fabricated on the 300ºC SnO_2 (most preferentially oriented films) exhibited the best performance, suggesting that the orientation of these films may play an important role in determining the final solar cell performance.

3.5.2.2 SnO_2 by Reactive Sputtering of a Sn Target

As indicated previously the material properties of reactively sputtered SnO_2 films were not thoroughly investigated, rather based on the results from films prepared from a SnO_2 target, a deposition temperature of 300ºC was chosen as "optimum" and subsequently all reactively sputtered SnO_2 films were deposited at this temperature. Using these conditions a series of devices were fabricated using Cd_2SnO_4/SnO_2(reactive sputtering) as the substrate, where the thickness of the SnO_2 was varied (125, 250, 500, and 1000Å). Light J-V for representative devices are shown in Fig. 17, with a list of their solar cell parameters provided in table 6.

Table 6. Solar Cell Parameters for CdTe Cells Fabricated on Cd_2SnO_4/SnO_2(Reactive Sputtering) Substrates

SnO_2 Thickness [Å]	V_{OC} [mV]	FF	J_{SC} [mA/cm^2]	R_{SERIES} [Ω-cm^2]
125	710	0.53	22.41	5.15
256	730	0.58	22.37	2.65
500	800	0.69	22.80	1.22
1000	825	0.70	23.73	0.90

The V_{OC} gradually decreases as the SnO_2 thickness is decreased, spanning a range of over 100 mV. This decrease in V_{OC} indicates a degradation in the junction properties of the cells as the SnO_2 is thinned. Although not yet verified, it is believed that part of the observed V_{OC} loss, is poor collection at long wavelengths (monochromatic J-V measurements are underway to further evaluate these devices). The FF also shows a decreasing trend with decreasing SnO_2 thickness ranging from 0.70 to 0.53, presumably due to poor junction characteristics (poor collection). However, the FF is also affected by a consistent increase in the series resistance (with decreasing SnO_2 thickness). It is interesting to note that the light and dark series resistances (estimated from the slope of the J-V characteristics displayed in Fig. 18) are approaching the same value for the two larger SnO_2 thicknesses, however, for the two smaller thicknesses, the dark series resistance is clearly higher than the light. It is possible that the "thin" SnO_2 films interact with the CdS affecting its resistivity or forming a "barrier" at the SnO_2/CdS interface leading to the

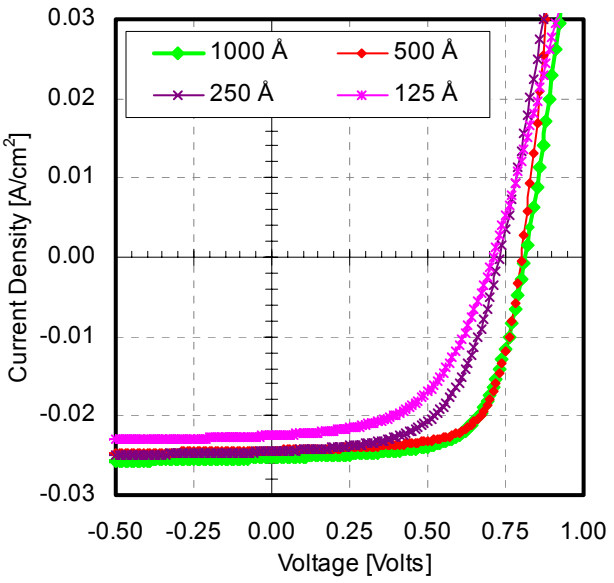


Figure 17. Light J-V characteristics for cells with reactively sputtered SnO_2 as a buffer

observed increase in the series resistance. On the other hand the light shunt resistances of all devices have exceeded 1000 Ω-cm^2, suggesting that shunting is not a limitation in these cells.

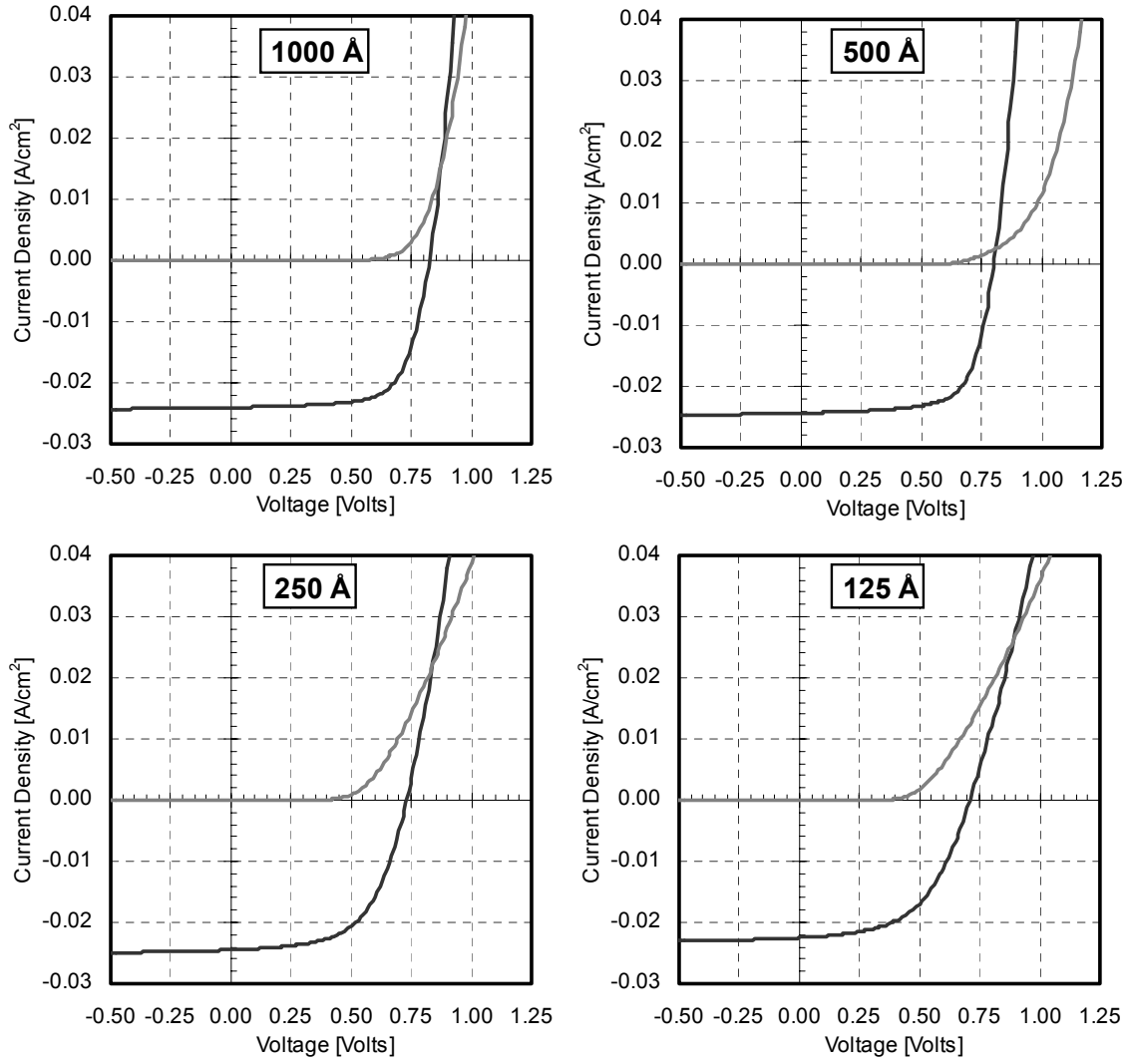


Figure 18. Dark and light J-V for CdTe cells fabricated using reactively sputtered SnO_2 of various thicknesses as a buffer

4.0 IMPROVING MANUFACTURABILITY – DRY PROCESSING

One of the tasks being addressed under this project deals with improving the manufacturability of CdTe devices. In order to address this issue, a vapor $CdCl_2$ heat treatment is being studied with the ultimate objective to develop a completely "dry" fabrication process. In addition, a submodule size reactor capable of coating 10 x 10 cm^2 moving substrates, has been brought on-line, in order to study/identify critical issues associated with the deposition of CdTe, that can help bridge the gap between small area devices and module efficiencies.

4.1 Large Area Deposition System

Work on the large area deposition system has to-date focused on troubleshooting the process and making the necessary adjustments/modifications in the source and substrate holders/heaters, in order to achieve uniform film deposition. A schematic of the CdTe chamber is shown in Fig. 19. The key components of the apparatus are three large area heaters and a transport mechanism for positioning/moving the substrates. The pyrolytic boron nitride (PBN) heaters are approximately 12 x 12 cm^2 in size. Two of these are used for substrate pre-heating and heating during the deposition; the third one is used for heating the source material[†]. The source material is supported in a large (12 x 12 cm^2) shallow, high density graphite boat. The temperatures are monitored using thermocouples in direct contact with the heaters. Depositions are carried out under stationary ambient conditions. The substrate holder is removable allowing for the coating of a single large or four small size substrates.

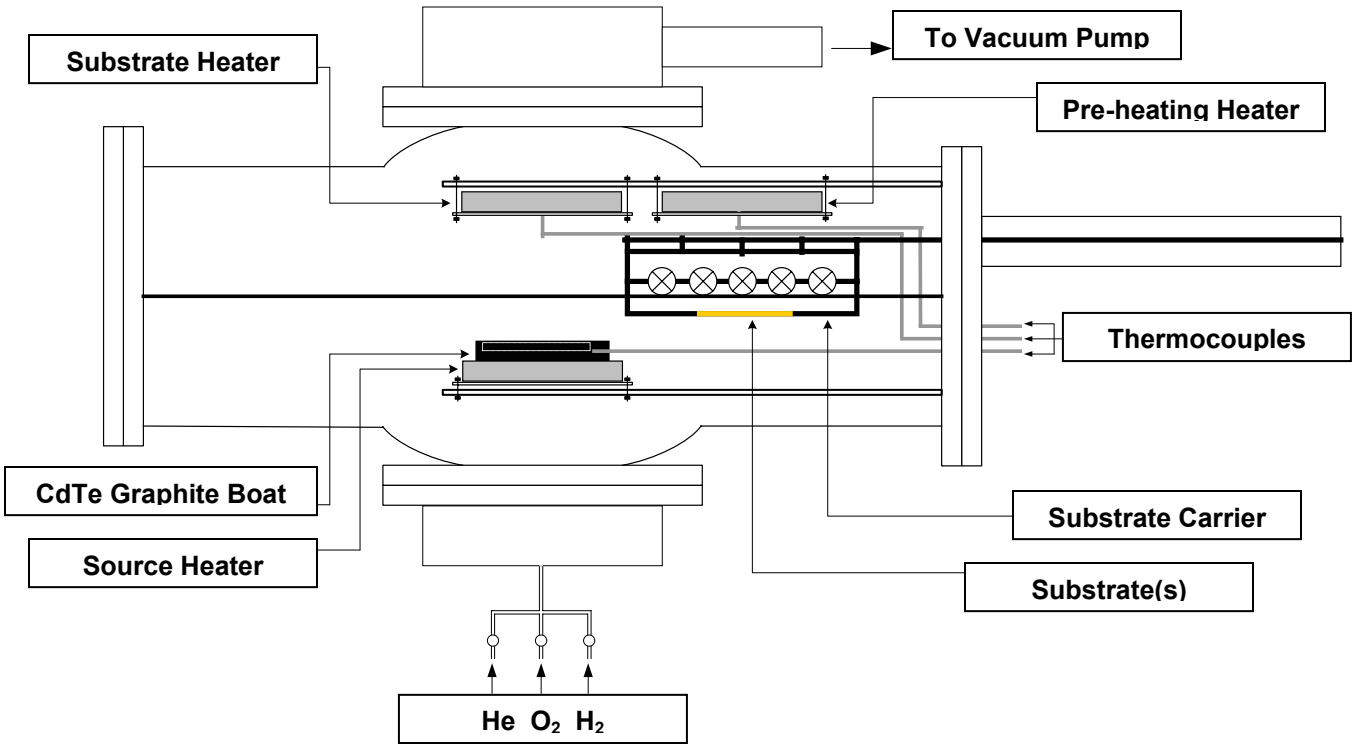


Figure 19. Schematic of the large area CSS deposition system

[†] A quarterly report discussed the fact that some of these heaters malfunctioned and had to be replaced. Heater reliability remains a serious issue and it is expected that the current heaters will be replaced.

Initial depositions were carried on stationary small substrates, however, after achieving reasonable thickness uniformity (within ±10%), subsequent depositions were carried out with substrate motion. Presently the process has been adjusted for deposition rates in the 2-3 μm/min range. Initial devices have reached V_{OC}'s up to 830 mV and FF's of 68%. Occasionally the CdTe films contain pinholes which is a key issue to be addressed in future work.

4.2 Vapor Chloride Treatment

The vapor $CdCl_2$ process has been described in detail in a previous report [1]. Cells are heat treated in a 2-zone furnace where the temperatures of the sample and $CdCl_2$ can be controlled independently. The $CdCl_2$ vapors are transferred to the sample zone using a carrier gas. The primary focus of this activity has been to improve the manufacturability of this process. The use of vapors eliminates the need for wet processing (i.e. the coating of CdTe using $CdCl_2$ solutions), and shorter annealing times can improve the overall throughput. The ambient (carrier gas) has also been varied and as indicated previously it has been found that the presence of O_2 during this process lead to improved device performance. Although most cells are being treated in O_2 ambient, experiments using inert or H_2 ambient are also being carried out. It should be noted that temperatures and annealing times for this section are *approximate*, especially where the annealing times are below 2-3 minutes[†].

4.2.1 The Effect of Substrate Temperature

Unless otherwise stated all results discussed in this section are for vapor treatments carried in the presence of O_2. An important process parameter is the substrate temperature; typical "optimum" temperatures for the $CdCl_2$ heat treatment are around 400ºC. In an effort to shorten annealing times higher substrate temperatures were utilized. In general, increasing the substrate temperature above the typical 390-410ºC range, lead to lower solar cell performance, in some cases the losses were significant (specifically when annealing times were in the 10-20 minute range). Figures 20 and 21 show the V_{OC} and FF for a batch of cells heat treated at different temperatures for different annealing times. Although the trends in this set of experiments are not very consistent, it is encouraging to note that two of these cells exhibited V_{OC}'s and FF above 800 mV and 65% respectively for annealing times less than 5 minutes (460 and 500ºC). The light J-V data for the devices heat treated at 500ºC are shown in Fig. 22. These clearly show that the low FF's for the 1 and 5 minute annealing times are due to non-ohmic back contacts. As all of the cells shown in Figs 20 and 21 have been contacted *without the standard CdTe etch* (in bromine/methanol), it is believed that some of the observed "inconsistencies" are due to irreproducibility related to the back contact, possibly due to oxide formation on the surface of CdTe.

The most difficult aspect of this process is associated with controlling the process parameters, in particular during the heating up period. To simplify things the substrate temperature is always kept slightly higher than the $CdCl_2$ temperature in order to keep $CdCl_2$ from depositing on the sample surface. Also, O_2 is allowed to flow into the reactor prior to the start of the annealing process (i.e. at room temperature). In cases where the annealing process is less than 2 minutes (i.e. the time period from the instant the substrate has reached the required temperature until the heaters have been switched off), the heating up process may be as long as the heat treatment itself. When the annealing process is a few seconds, then the heating up period is significantly longer than the actual process. It therefore becomes increasingly difficult

[†] High temperatures combined with short annealing times make it difficult to precisely control the annealing temperatures due to overshoot.

to reproduce results for such conditions although attempts have been made to do so. An example where the annealing times have been kept very short (1 minute or less) is shown in Figure 23. It must be emphasized that these results should only serve as an indication that short annealing times are feasible for this process; it is emphasized that the heating up portion of the process is of the order of 2 minutes, and therefore the samples are within approximately 20ºC of the indicated annealing temperature for times longer than those shown in this figure as "annealing times". In a manufacturing setting, this may not be an issue as the modules will be at elevated temperatures following the CdTe deposition, at which time they can enter a vapor $CdCl_2$ chamber where the ambient ($CdCl_2$ vapors and O_2 concentration) can be maintained at a steady state.

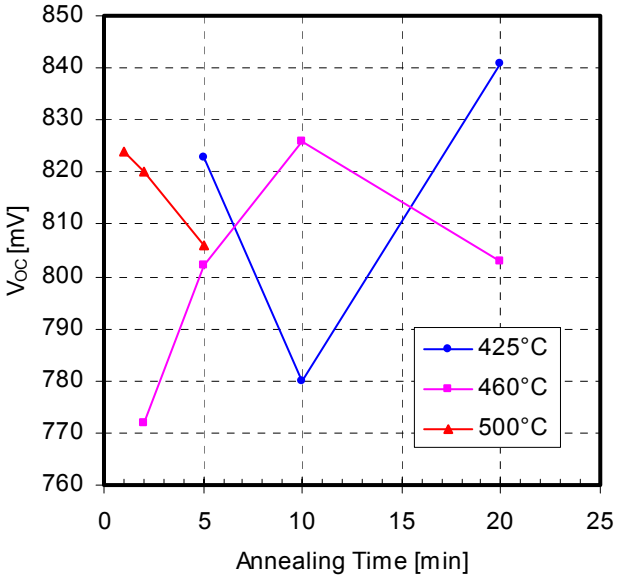


Figure 20. V_{OC} of vapor treated CdTe cells for temperatures as high as 500ºC

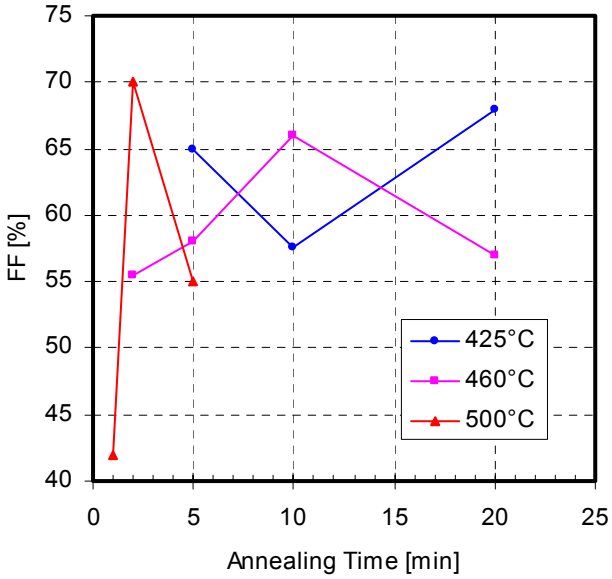


Figure 21. The FF of the cells shown in Fig. 20

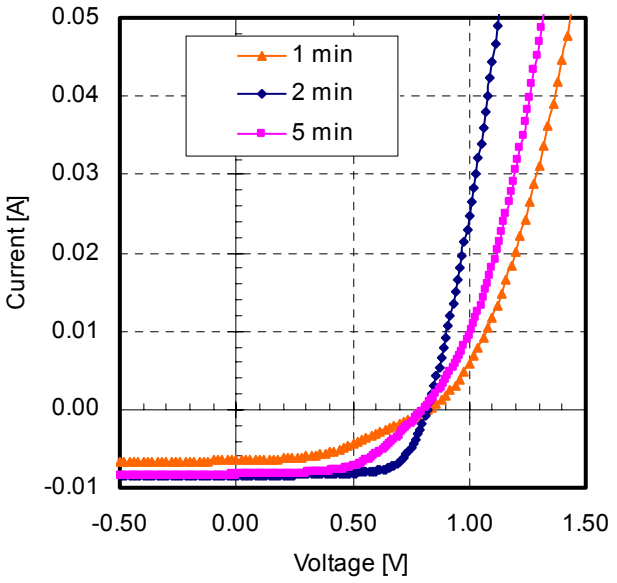


Figure 22. Light J-V for the 500ºC cells of Figs 20 and 21

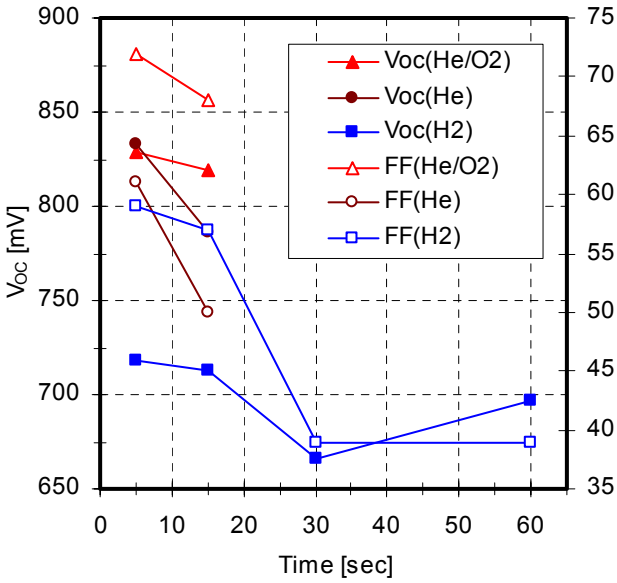


Figure 23. V_{OC} and FF for cells vapor treated for times less than 1 minute

4.1.3 Device Analysis

Representative cells form the currently "optimum" conditions based on He, H_2 and O_2 ambient are listed in table 7; these represent cells with the best V_{OC}/FF combinations. It should be noted that these results were obtained *without the use of a chemical etch* prior to the back contact formation. One of the most consistent results with regards to the devices treated in H_2 was the limitation of V_{OC}'s below the 800 mV mark.

Table 7. V_{OC} and FF of to-date best vapor treated CdTe cells

Ambient	V_{OC} [mV]	FF
He/O_2	840	0.73
He	830	0.65
H_2	790	0.68

Figure 24 shows the dark J-V for theses devices along with J_{SC}-V_{OC} data. Based on these the lower V_{OC} for the device vapor treated in H_2 is lower due to its higher dark current (J_O). The A factor for these device was also higher (see table 8). These results suggest that the junction properties are influenced significantly by the ambient utilized during the treatment. It is not clear at this time how H_2 has a negative impact on the junction (i.e. mechanism leading to the higher J_O). The use of O_2 during the $CdCl_2$ treatment has been previously found to influence the extent of interdiffusion between CdTe and CdS, and therefore the junction properties [9]. However, it should be noted that using SR measurements to estimate/compare the CdS thicknesses in the cells studied during this work, no effect on the final thickness of CdS due to the presence of O_2 was identified. It is believed that the reason for this is the fact that the cells discussed here were fabricated at high temperatures and do not undergo any grain enhancement or extensive interdiffusion during the $CdCl_2$ process.

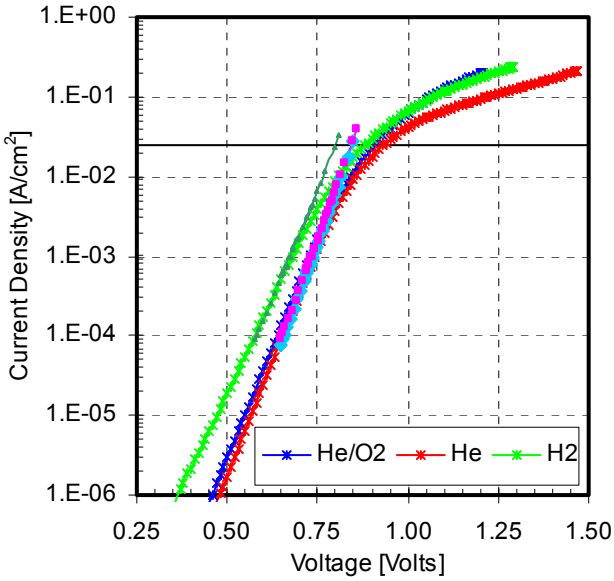


Figure 24. Dark J-V for devices vapor treated in various ambients; J_{SC}-V_{OC} data are also shown for currents in the range of 10^{-4} to $3x10^{-2}$ A/cm^2

The same devices were also characterized using monochromatic light J-V measurements. Figure 25 displays plots of the effect of the wavelength on the FF (a), as well as the normalized J-V data for the three cells (b through c). As in devices discussed in a previous section, the FF of all cells shows a strong dependence on the wavelength, suggesting that it is limited due to inefficient collection. The FF of the device annealed in H_2, is overall lower than the other two devices, as strongly absorbed light results in lower FF's than the other two cells, presumably due to increased interface recombination.

Table 8. A and J_O values calculated from J_{SC}-V_{OC} measurements

Ambient	H_2	He	He/O_2
A	1.62	1.37	1.38
J_O [A/cm^2]	6.00E-11	5.00E-13	5.00E-13

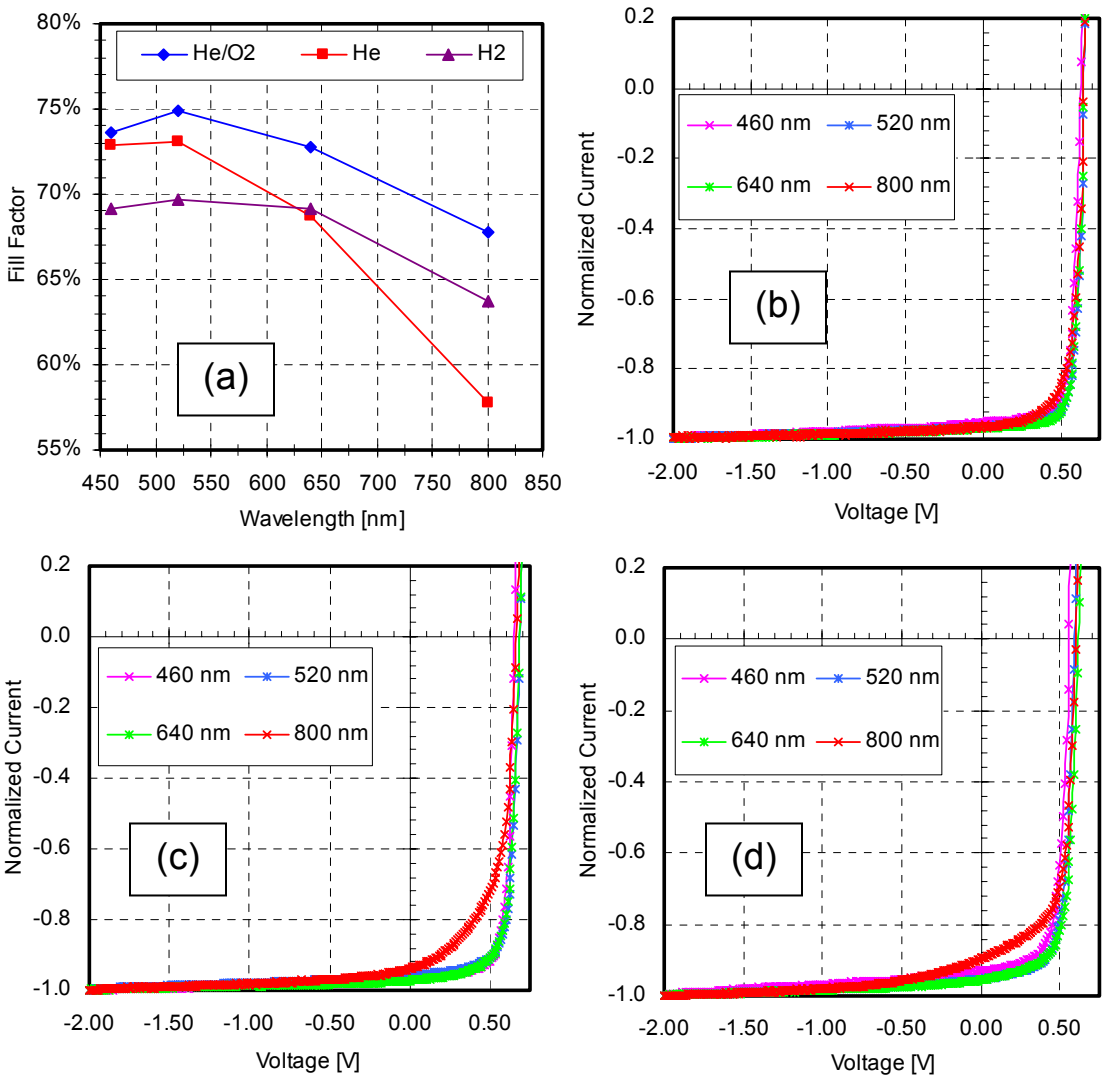


Figure 25. (a) FF vs. wavelength; monochromatic light J-V for devices vapor treated in (b) He/O_2, (c) He, and (d) H_2

5.0 BACK CONTACTS - Sb_2Te_3

The use of Cu in the formation of effective CdTe back contacts is well known. However, the issue of stability and the belief that Cu plays a key role in observed device degradation has lead to efforts to develop effective Cu-free back contacts. One approach that produced very encouraging results has been based on the application of Sb_2Te_3 by sputtering[10]. This type of contact has been investigated previously at USF. As indicated in previous reports this process has presented many challenges including a significant degree of scattering in solar cell performance. During the first year of this project, a series of devices were fabricated using Sb_2Te_3 sputtered under conditions previously found to be "optimum" for this approach[1]. Substrates prepared at USF as well as material received from First Solar, Inc. were contacted with Sb_2Te_3. Figure 26 shows I-V data for USF (left) and FS (right) CdTe. All devices exhibited "roll-over" indicating that the Sb_2Te_3/CdTe interface results in the formation of barrier. This set of J-V data represent the typical device performance obtained using Sb_2Te_3 since the start of this effort. However, this was the first time that CdTe from two sources was utilized. Although the contact fabrication procedures were similar for FS and USF material it appears that on average FS devices outperformed USF cells. It is obviously expected that the properties of CdTe will have an effect on the back contact properties, however, regardless of this difference the best performance characteristics obtained for First Solar material were FF's in the mid to upper 60's and V_{OC}'s in the 600-730 mV range; both quantities are considerably lower than what can be obtained using a different back contact process such as the doped graphite, or sputtered Cu_XTe. The results shown here represent the final set of experiments carried out using Sb_2Te_3 as it is believed that all possible parameters were investigated without any indication that this material can form an effective back contact to CdTe.

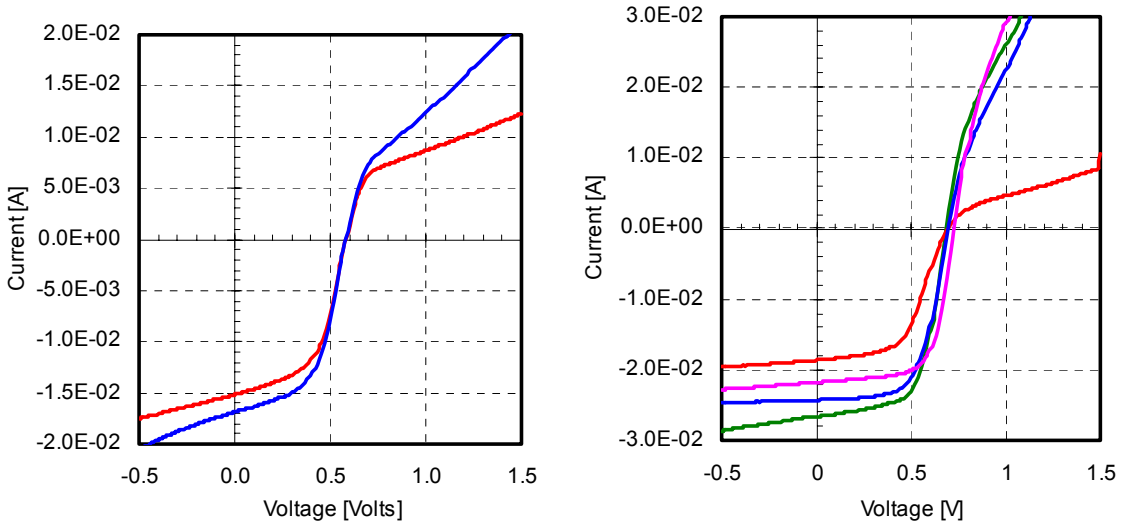


Figure 26. Light J-V for Sb_2Te_3-contacted cells using USF CdTe – left, and First Solar Inc. CdTe - right

6.0 STABILITY STUDIES – THE EFFECT OF THE $CdCl_2$ HEAT TREATMENT

6.1 Experimental/Device Details

One of the major tasks of this project deals with long term stability issues. During the first year an experiment was designed to evaluate the impact of the $CdCl_2$ heat treatment on CdTe solar cell stability. The objective was to light soak devices processed under various $CdCl_2$ heat treatment conditions that include both optimum and non-optimum performance. The only variable varied in the device fabrication process was the annealing temperature which was sufficient to allow for significant variation in device performance. In most cases, whether the heat treatment is carried out in the presence of vapors or simply $CdCl_2$ solution, the CdTe cells are heat treated at temperatures around 400ºC. For this work the cells were heat treated at temperatures ranging from 360 to 400ºC. The performance data are shown in Fig. 27. The red lines represent maximum and minimum performance data and the blue lines averages; solid lines are for V_{OC} and dotted lines for FF; averages are based on a minimum of nine cells for each condition shown in Fig. 27 (1 witness sample; 4 light soaked @ V_{OC} and 4 @ J_{SC}). As seen from this figure the V_{OC} is only slightly affected by the annealing temperature as in nearly all cases it remains above 800 mV. However, the FF is affected significantly over this range of processing conditions with the average value dropping to values as low as 60%. Higher annealing temperatures (up to 420ºC) resulted in FF's in the 30-40% range (not shown in Fig. 27), and such samples were not included in this study, not only due to their low performance but also due to significant scattering in the data. The group of devices depicted here was deemed adequate for the experiment and they were subsequently mounted inside a vacuum oven where they were light soaked.

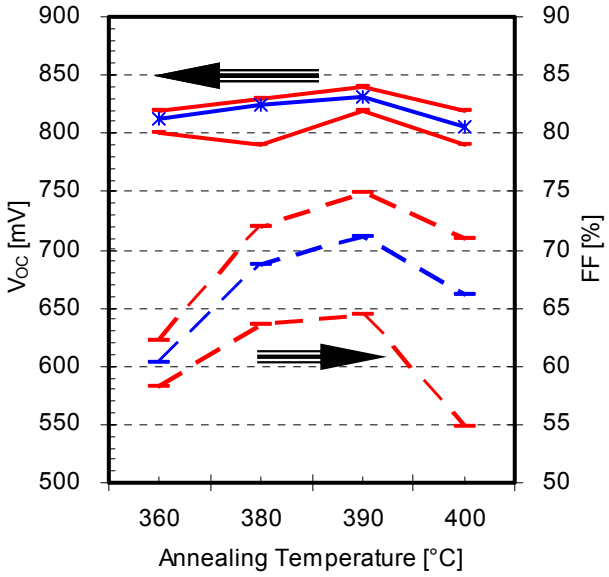


Figure 27. Performance data for cells included in the $CdCl_2$/stability study

The light soaking set up is shown in Fig. 28. The sample "platform" consisted of a Cu plate that was water cooled using city water. The Cu-plate was coated with a thermal compound (used to mount high power electronic components to heat sinks), which was covered with a thin insulating film to avoid direct contact between the cells and the thermal compound. The cells were pressed firmly into the film/thermal compound using an LOF glass plate. Not shown in the above schematic are three CdTe substrates used as temperature sensors. These substrates were bonded to thermocouples and placed at three different locations on the plate (mounted the same way as the devices under test). The thermocouple signals were fed back to temperature controllers which were used to control water solenoids to turn the cooling water on and off. The entire set up as depicted in Fig. 28 was placed inside a vacuum oven. Prior to the start of the light soaking cycles, the oven was evacuated and back filled several times with N_2. The oven was eventually backfilled with N_2, and a small constant flow of N_2 was maintained through the oven; using a pressure relief valve the oven was kept at a slightly positive pressure. The light soaking process was a 4 hour ON/4 hour OFF cycle in order to identify any transient mechanisms of this order. The light intensity varied by approximately ±15% over the area of the

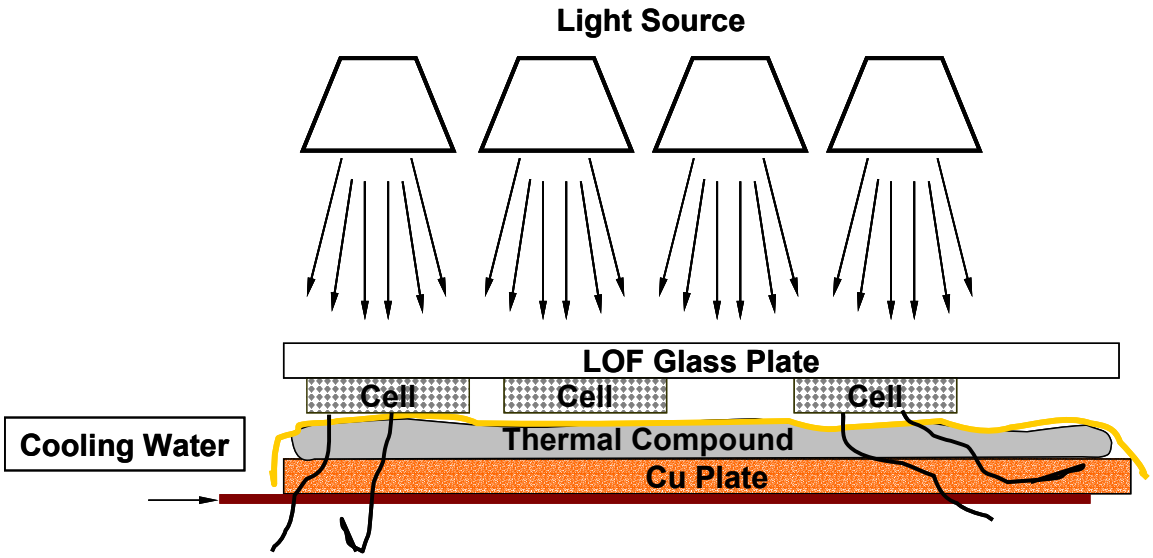


Figure 28. Schematic diagram of the light soaking stage

sample stage. The temperatures on the platform could reach 55-65ºC depending on the location of the thermocouples. At this time the temperature variations could not be eliminated without major modifications to the platform. This is an issue to be addressed in future experiments.

Eight (identical) cells were stressed at each temperature. Four were held at open-circuit (OC) and four at short-circuit (SC) conditions. Current-voltage measurements (dark and light) were taken during the first and the last hour of the ON/OFF cycles. The cells were light soaked for approximately 1000 hours (i.e. 1000 hours under light and 1000 hours in the dark). The following sections present the results of this study. Due to the repetitive nature and the large amount of data/graphs, most of the J-V characteristics are included at the end of the CdTe part of this report in section 7.0.

6.2 Results

6.2.1 Devices $CdCl_2$ Heat-Treated @ 360ºC - Light Soaked @ Open-Circuit

6.2.1.1 Performance Data

Figure 29 shows the V_{OC} and FF for four cells (two cells per graph) held at OC and light soaked for 1000 hours[†]. These cells were $CdCl_2$ heat treated at 360ºC which is not an "optimum" processing condition. The V_{OC} for all four devices shows similar behavior/trend during the 1000 hours of light soaking. It appears to slightly increase initially (during the first 10 hours), then remains essentially constant for 400-500 hours, but subsequently appears to exhibit a decreasing trend during the last portion of the 1000 hour light soaking period. *It should be noted that the data shown in Fig. 29 and in all similar figures were taken at operating temperatures.* The V_{OC} measured during the last hour of the ON cycle is always lower than what is measured during the 1st hour; the reason for this is the fact that the cell temperature tends to increase gradually during the ON cycle. The FF for the same devices behaves

[†] Cells on the same graph were fabricated on the same substrate.

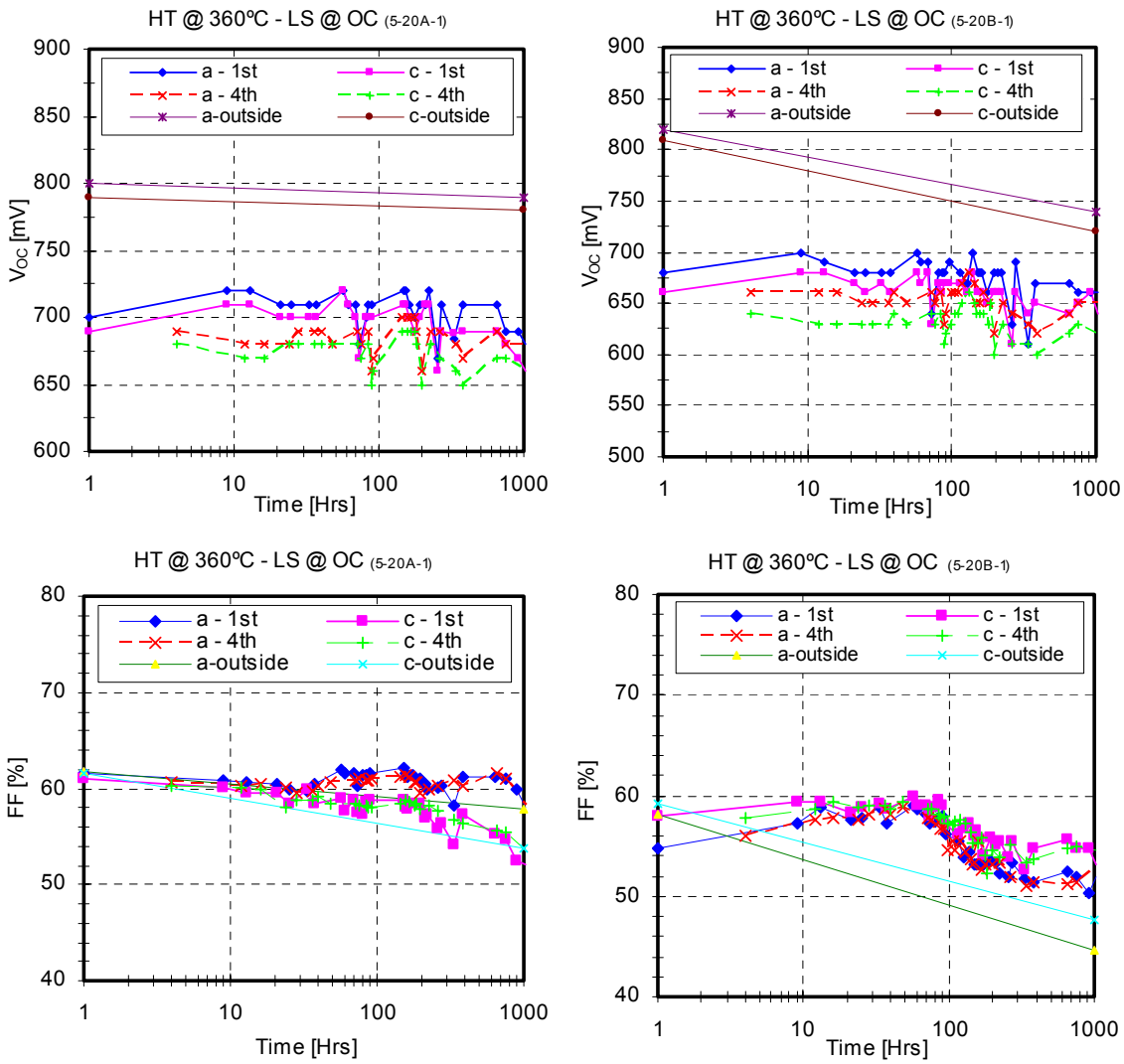


Figure 29. V_{OC} and FF of cells $CdCl_2$ heat treated @ 360ºC, and light soaked @ OC conditions; solid lines: 1st hour of ON cycle; dotted lines 4th hour of ON cycle

differently. In one case (left) it decreases gradually during the first 40 hours, then increases for a period of about 100 hours, and during the latter stages of the entire process seems to follow a decreasing trend. The FF of the second set of devices (right) does not undergo an initial decrease, but rather increases for approximately 100 hours and then shows a gradual decrease and appears to be leveling off during the latter stages of the 1000 hour period. In general, although the V_{OC} trends/behavior observed for the two sets of devices is similar, the FF seems to exhibit subtle differences, at least initially, that require additional analysis and understanding. It should be noted that although all cells in Fig. 29 were processed under "identical" conditions, small variations in parameters such as the CdTe thickness (5-10%) may exist; the extent to which they are responsible for what is observed above is not clear at this time.

6.2.1.2 Dark and Light J-V

Dark and light J-V data for the devices depicted in Fig 29 are shown in Fig. 7.1 ***Section 7.0***. The various graphs include J-V data taken initially (prior to the light soaking experiment and at

room temperature), and after 100 and 1000 hours of light soaking. Additional J-V data may also be included in order to demonstrate when the most significant changes took place.

The Ln(J)-V data shows that initially all samples exhibit qualitatively similar characteristics; both the slope and intercept (A and J_O) are very similar and well within experimental variations. They also exhibit very similar Ln(J)-V after 1000 hours of light soaking, where the dark current at low voltages has increased considerably (region "A"). This increase was in the past labeled as a "shunt" component of the current, however, a close examination of the light J-V in the 1-2 volts reverse bias range (region "E"), indicates that there is no significant shunting in these devices; at least not enough to account for the current measured in region "A". *It is therefore suggested that the bulk of the current increase in region "A" is due to increased recombination*. With regards to this increase in recombination current, it seems that it is of the same magnitude in all cells, with the only difference being in the timing of this change. The sample labeled "5-20B-1" (Fig 7.1 – right), has reached high recombination current levels within the first 100 hours with no significant changes thereafter, while the sample labeled "5-20A-1" had considerably lower currents at the 100 hour mark; however, it eventually "caught up" with "5-20B-1" after 1000 hours. This difference in the "timing" of the observed dark J-V coupled with the fact that eventually the cells reach similar levels of dark currents, suggests that a processing variation has possibly accelerated the increase in recombination in some of these cells.

Additional changes observed in these samples are labeled as regions "B", "C" and "D". Regions "B" and "C" mark the same change – an increase in the dark current at high voltages. Initially, the cells appear to have their forward current limited as seen in region "B". This is a region where series resistance and high injection effects are typically dominating the J-V behavior, however, in this case the limitation is due to a different mechanism. The entire (linear) J-V characteristic is *shifted* to higher voltages, leading to an apparent increase in the turn-on voltage. This is believed to be caused by a "barrier" formed at the front of the device i.e. between SnO_2/CdS and CdTe, or by CdS (to be discussed below). This behavior has been seen previously in USF devices and it was then indicated it does not have an effect on the light J-V of the cells[1]. However, as shown in Fig 7.1, after light soaking the mechanism responsible for the unusually low current in region "B" (or "C") is no longer present. It should be noted that unlike the increase in recombination currents discussed above (region "A"), in this case the timing is very similar, i.e. the bulk of this change has taken place within the first 100 hours for all cells in this set. The last significant change in the J-V characteristics of these cells is marked as region "D". It appears from the data that the slope of the light J-V in this region (which can be used to approximate the series resistance of the devices), is larger initially and begins to decrease under light soaking. However, a comparison of the light J-V in region "D" for the measurements taken at 100 and 1000 hours, reveals that the apparent series resistance at 1000 hours is higher i.e. the initial trend of decreasing series resistance has been reversed (partially). It should be noted that the slope of the dark J-V at high currents is also following the same trend after the entire curve has shifted to lower voltages.

In summary, the devices $CdCl_2$ heat treated @ 360ºC have undergone significant changes during the 1000 hours of light soaking:

(a) a *shift* of the dark J-V characteristics to lower voltages (regions "B" and "C") which could be related to changes in the properties of the CdS and/or the presence of a barrier at the front of the device.
(b) an increase in the recombination current (region "A") suggests an increase in the concentration of defects responsible for the current transport at the junction.
(c) an eventual increase in series resistance (both light and dark) most likely associated with compensation taking place within the bulk of the semiconductors.

Finally, after 1000 hours of light soaking all samples appear to exhibit similar behavior; however, the changes during the light soaking process are not concurrent, which seems to correlate with the apparent inconsistent trends observed in the behavior of the FF. Subsequent sections will summarize these changes (using the regions labeled "A: through "E") for the various light soaking conditions/samples.

6.2.2 Devices $CdCl_2$ Heat-Treated @ 360ºC - Light Soaked @ Short-Circuit

6.2.2.1 Performance Data

Figure 30 shows the V_{OC} and FF for cells from the same substrates as the ones in the previous section; the devices here were light soaked at SC. It should be noted that one of the devices from substrate "5-20B-1" failed and only V_{OC} data for the first 100 hours are included in the graph[†].

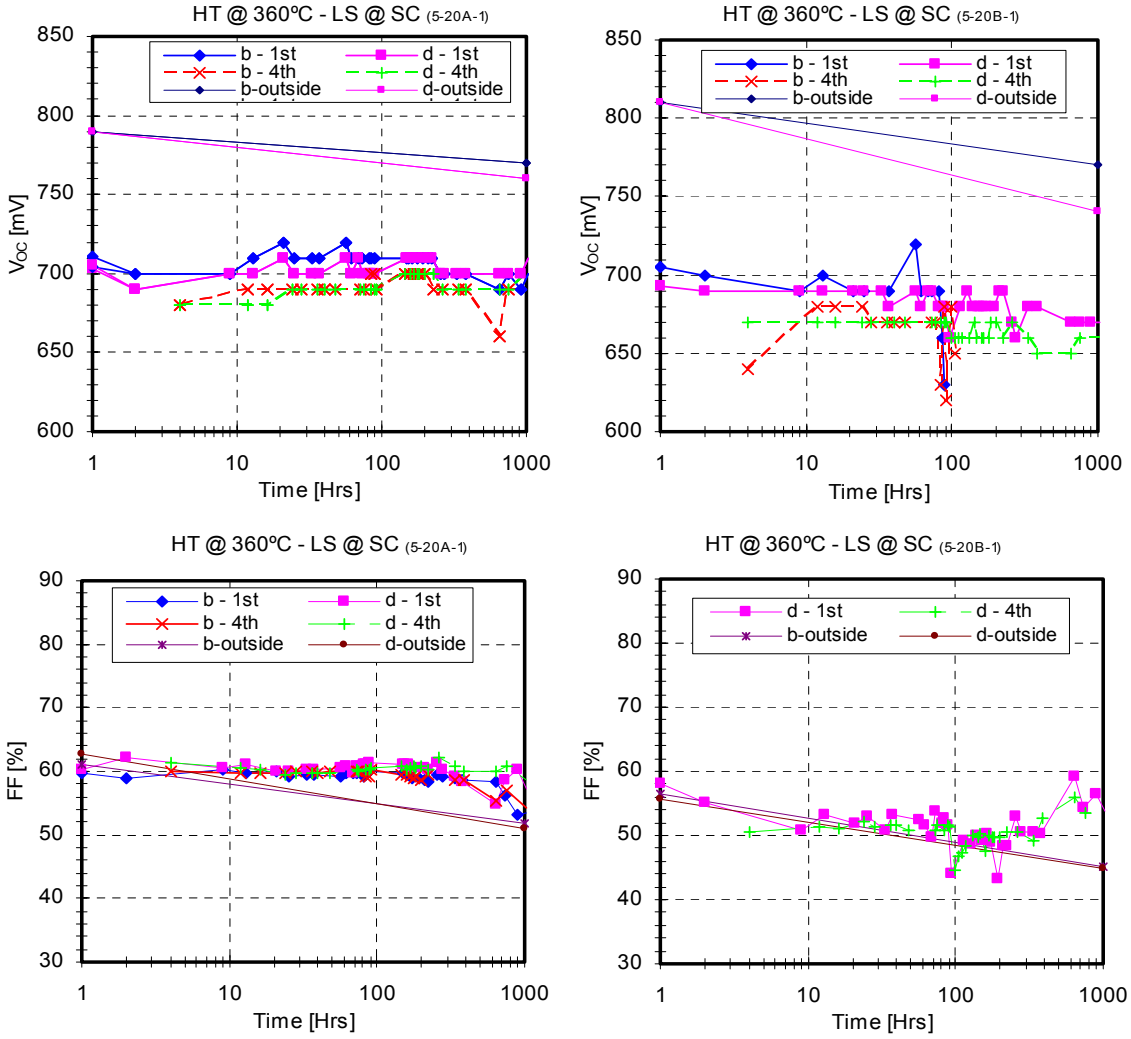


Figure 30. V_{OC} and FF of cells $CdCl_2$ heat treated @ 360ºC, and light soaked @ SC conditions; solid lines: 1st hour of ON cycle; dotted lines 4th hour of ON cycle

[†] Additional discussion on samples that exhibited catastrophic failure is provided in another section.

In general, the V_{OC} of both devices exhibits similar trends as the ones observed for the cells light soaked at OC, with the 1st hour measurement yielding higher values than the 4th hour due to an increase in the cell operating temperature. It also appears that although the V_{OC} for sample "5-20A-1" (left) remains essentially unchanged during the 1000 hours, the V_{OC} of the second sample ("5-20B-1" – right) seems to exhibit a steady decrease during the last 400 hours. The FF for the two samples exhibits a different trend (as was the case for the devices held at OC). The FF of sample "5-20A-1" is unchanged for one of the two cells, with the second device exhibiting a gradual decrease during the last 200 hours. However, the FF of sample "5-20B-1" follows a trend that appears to be "the opposite" of that of the cells held at OC. In this case, the FF decreases during the early stages of light soaking (approx. 150-200 hours), and subsequently increases (200-1000 hours) to eventually reach its initial value. It should be again noted that the cells discussed to this point (i.e. $CdCl_2$ heat treated at 360ºC) were fabricated using "identical" fabrication conditions. However, based on the observed differences in their behavior during light soaking, it is reasonable to conclude that they are not quite "identical", which suggests that even small variations in processing can have significant impact on the long term behavior of these cells.

6.2.2.2 Dark and Light J-V

The J-V data for the cells of Fig 30 (i.e. light soaked at SC) are shown in Fig 7.2 at the end of the CdTe section. The same regions "A" through "E" discussed earlier are also labeled in this figure.

Region "A": all devices exhibit an increase in the recombination current that after 1000 hours is similar in magnitude to what was observed for the cells held at OC. However, *during the first 100 hours the recombination current of the samples held at OC increased more rapidly*. Therefore, it appears that all devices are undergoing the same changes regardless of bias, with the SC condition simply delaying these changes.

Regions "B" and "C": the entire J-V characteristics are again *shifted* to the left within the first 100 hours, with a subsequent increase in the slope i.e. in the series resistance of the cells. This *increase in the series resistance appears to be more prominent for the cells held at SC* than it was for those held at OC.

Regions "D" and "E": changes in the light series ("D") and shunt ("E") resistances are similar to what was observed for the OC conditions and no significant differences can be identified.

The most significant differences between the OC and SC conditions appear to be:

(a) the rate of increase in the dark current is initially (first 100 hours) slower for the cells held at SC.
(b) the light series resistance of the cells held at SC appears to be increasing to greater values than that of the cells held at OC.

6.2.3 Devices $CdCl_2$ Heat-Treated @ 400ºC - Light Soaked @ Open-Circuit

6.2.3.1 Performance Data

Figure 31 shows the performance data (V_{OC} and FF) for cells light soaked at OC, and $CdCl_2$ heat treated at 400ºC, which is typically the "optimum" annealing temperature for CdTe cells[†]. As in the previous data sets presented above the device characteristics were measured during the 1st and 4th hour of the light cycle. The V_{OC} remains unchanged for the first 100 hours, but beyond that it exhibits a gradual decrease for all devices. The FF trend is essentially identical

[†] For the samples included in this study 390ºC yielded better performance (see Fig 27).

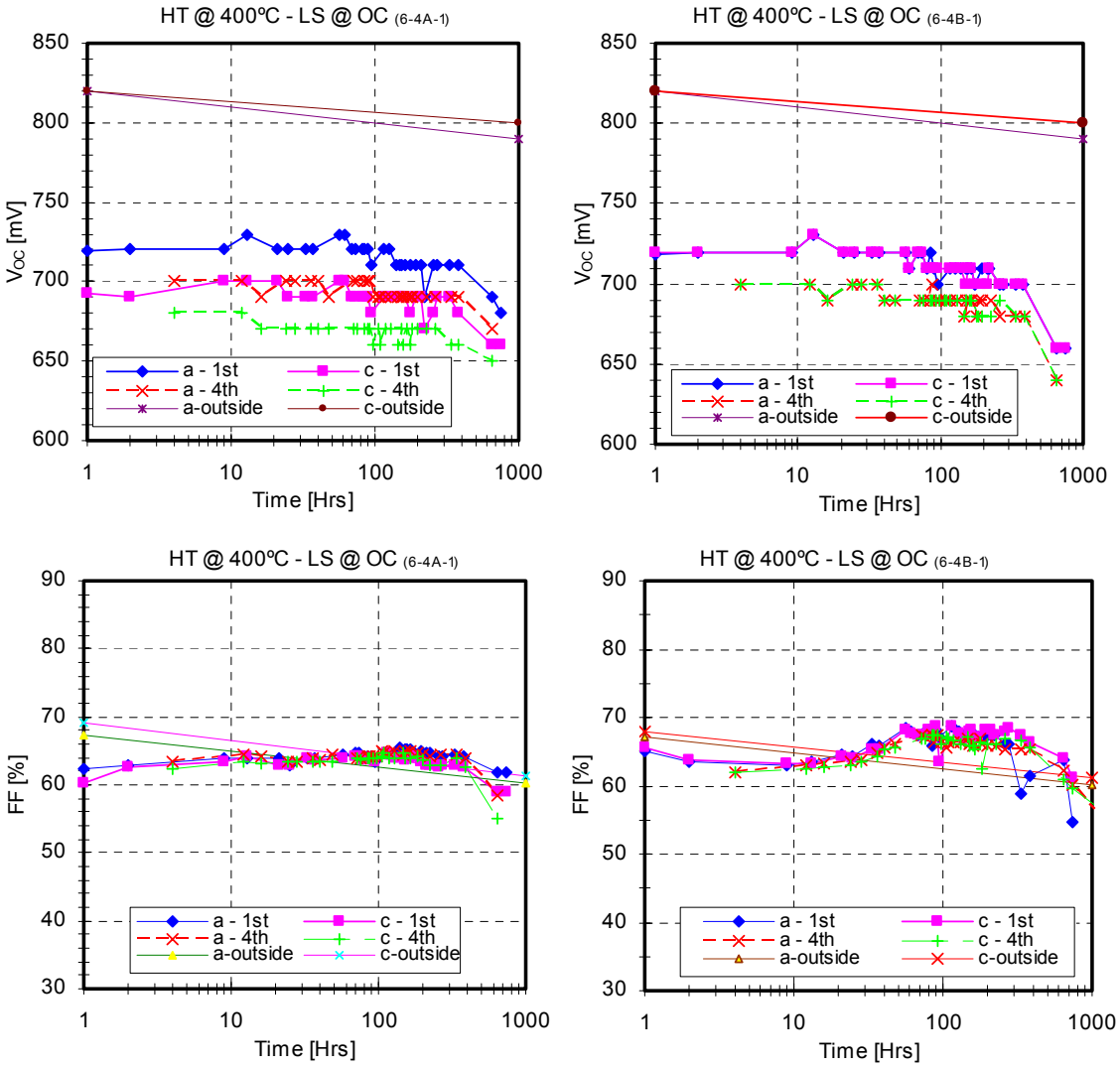


Figure 31. V_{OC} and FF of cells $CdCl_2$ heat treated @ 400ºC, and light soaked @ OC conditions; solid lines: 1st hour of ON cycle; dotted lines 4th hour of ON cycle

for all devices, if one excludes the first 10 hours of sample "6-4B-1" (right); after an initial increase reaching a maximum in the 100-200 hour range, subsequently the FF exhibits a decreasing trend.

6.2.3.2 Dark and Light J-V

Figure 7.3 displays the dark and light J-V characteristics of the samples $CdCl_2$ heat treated at 400ºC and light soaked @ OC. The changes in the regions labeled "A" through "E" are qualitatively similar among all cells displayed in this figure; they are also similar to what was observed for the devices held at OC but $CdCl_2$ heat treated at 360ºC.

Region "A": the increase in the dark current (recombination component) is similar for three of the devices displayed but one. The current of sample "6-4A-1"/left increased considerably after 1000 hours, but is about an order of magnitude lower than the other three devices. The same cell at 100 hours exhibited considerably lower recombination current.

Regions "B" and "C": in all cases the entire J-V curves "shift" to lower voltages during the first 100 hours, with a subsequent increase in their slope indicating an increase in the dark series resistance. It should be noted that it is not possible to determine whether this observed

increase of the series resistance is a change that begun at the start of the light soaking process, as it would be masked by the *shift* of the J-V to higher voltages. However, based on the fact that the light series resistance (slope in region "D") does not begin to increase until after the first 100 hours, one can reasonably conclude that the mechanism responsible for this change (both dark and light) is initially insignificant or simply does not take place until the later stages of the light soaking process.

Regions "D" and "E": Changes in the light series resistance (region "D") have already been discussed above, while with the exception of one device none of the cells exhibit any appreciable amount of shunting.

6.2.4 Devices $CdCl_2$ Heat-Treated @ 400ºC - Light Soaked @ Short-Circuit

6.2.4.1 Performance Data/Light and Dark J-V

The V_{OC} and FF of the cells $CdCl_2$ heat-treated at 400ºC and light soaked @ SC conditions are shown in Fig. 32. As the data indicates these cells exhibit the most consistent behavior with

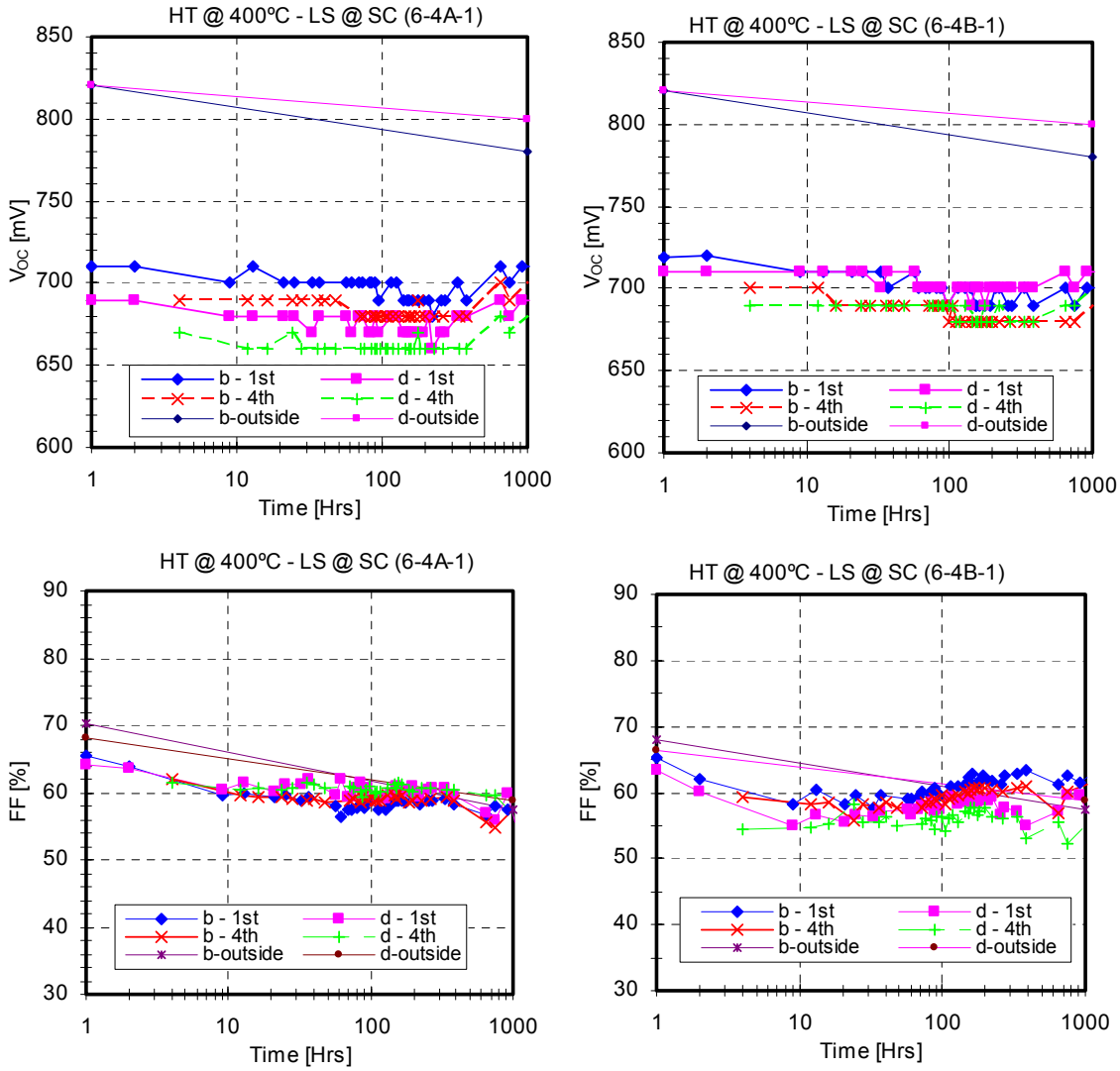


Figure 32. V_{OC} and FF of cells $CdCl_2$ heat-treated @ 400ºC, and light soaked @ SC conditions; solid lines: 1st hour of ON cycle; dotted lines 4th hour of ON cycle

regards to the general trends in both these parameters. After an initial decrease for approximately the first 100 hours, both the V_{OC} and FF appear to be recovering nearly reaching their initial values.

The J-V data for these cells are shown in Fig. 7.4. The qualitative changes undergone by these samples are in many ways similar to the previous samples and a detailed discussion is not necessary. However, this set of cells exhibit a rather unique behavior with regards to their dark currents. After 1000 hours of light soaking only two out of four cells exhibited an increase in their recombination current (region "A"), with the other two remaining essentially unchanged; A and J_O for sample "6-14A-1"/left for all practical purposes have not changed. Even though sample "6-14B-1"/right, does exhibit an increase in its recombination current, this is still about two orders of magnitude lower of what was observed for the OC conditions. It can therefore be concluded that samples *$CdCl_2$ heat-treated at the highest temperature (400ºC) and light soaked at SC exhibit a significantly lower increase in their dark currents*. The most challenging issue in this area of stability remains the identification of the specific defects and the changes taking place that lead to the observed behavior.

6.3 Summary of "$CdCl_2$/Stability" Results

The data and discussion provided above focused on the two extreme annealing temperatures used in this study. These two sets of data exhibited similarities as well as significant differences in their J-V characteristics during the 1000 hours of light soaking. The other two sets of samples (heat treated at 380 and 390ºC) are in good agreement with what was observed for the devices discussed in detail above. The samples heat treated at 380ºC behaved in a similar manner as the 400ºC ones, where those held @ OC exhibited an increase in their recombination currents, while those held at SC did not. Devices $CdCl_2$ heat-treated at 390ºC (which had the best initial performance) exhibited the smallest changes in their dark currents. Figure 7.5 in section 7.0 displays dark and light J-V data for these cells light soaked at OC and SC. It is clear that the increase in the dark current of these cells it is the smallest observed in all devices studied regardless of bias. The overall changes (averages that include all cells but the ones that appeared to completely short), after completion of the 1000 hours of light soaking are shown in Fig. 33. These data are from measurements taken at room temperature using the solar simulator. Cells heat treated at 380 and 390ºC exhibited the smallest changes in both their V_{OC} and FF. The change in V_{OC} is small *for all cells,* of the order of 5% or less, with the FF decreasing as much as 15-18% for the two worst cases.

Although some inconsistencies can be found in this set of data (most likely due unintentional to processing variations), it appears that

- Short-circuit conditions lead to smaller changes
- Cells fabricated near or at optimum $CdCl_2$ conditions exhibit the smallest overall changes
- In some cases the observed changes – in particular the increase in the dark current – were "delayed". However, after 1000 hours of light soaking the device characteristics were essentially indistinguishable.

With regards to the samples heat treated at 400ºC, it should be noted that this particular condition can yield state-of-the art devices. However, it can also lead to increase in data scattering, which is believed to be associated with CdS "over consumption" that can lead to the formation of local CdTe/SnO_2 junctions. As the data in Fig. 27 indicates, the spread in device performance increases with temperature. However, the observed changes in device characteristics seem to favor higher annealing temperatures. Although, at this time it is purely speculative, it is suggested that if the optimum performance can be shifted to higher $CdCl_2$

annealing temperatures, it is possible that the observed changes could be minimized and possibly eliminated.

Although, a correlation between device performance/characteristics and CdCl2 processing temperature was found, the findings of this experiment point to the complexities of the CdTe devices. The observed eventual degradation appears to be the result of more than one mechanism. Separating these mechanisms and isolating the particular defect(s)/processes responsible can lead to an improvement of the long-term stability of CdTe devices and modules.

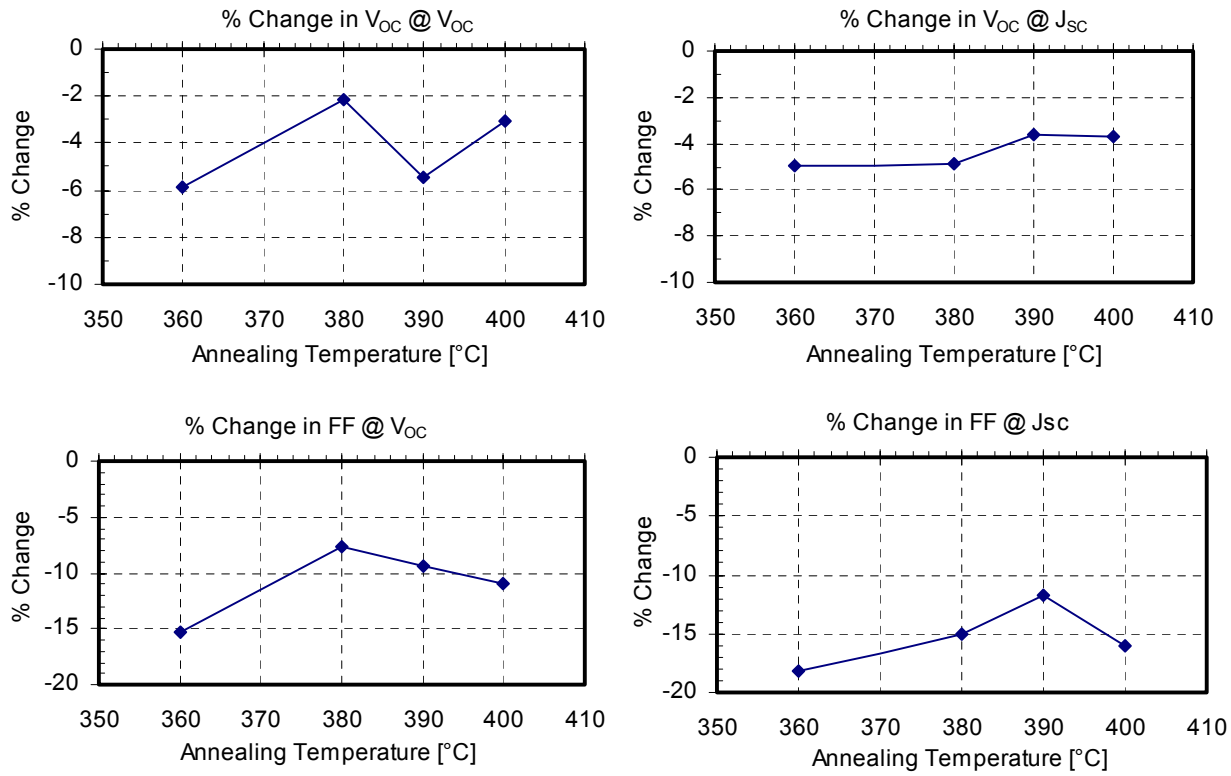


Figure 33. Changes in V_{OC} and FF after 1000 hours of light soaking. Data collected at room temperature using AM1.5 solar simulator

6.4 Failure due to Localized "Defects"

For the last few months the CdTe Thin Film Partnership Team has been focusing on "Micro-nonuniformity" issues, in order to determine whether the degradation observed in CdTe cells is due to weak micro-diodes (or microscopic defects). Table 9 lists the V_{OC} and FF for one of the cells that failed during the light soaking experiment discussed earlier. This is one of a handful of devices whose performance characteristics decreased dramatically and did not follow the general trends observed for the majority of samples. After the 1000 hours of light soaking, this cell was removed from the vacuum oven and re-measured to verify it had indeed failed. It was subsequently cut in half and the J-V for each half was measured. Based on the results listed in table 9, it appears that this particular cell failed because of a localized "defect" that caused the device to essentially short; more devices are currently being measured to determine whether they exhibit similar characteristics/behavior[†]. It therefore appears that the cause for at least some of the observed catastrophic behavior may not be due to the same mechanisms described in the sections above but rather a localized defect that shorts the device.

Table 9. V_{OC} and FF for a cell that exhibited catastrophic behavior during light soaking, but subsequently cut in halves and re-measured

	V_{OC} [mV]	FF
Prior to cutting	270	0.29
Top half after cutting	810	0.64
Bottom half after cutting	160	0.28

6.5 Light Soaking of Cu_XTe-Contacted Solar Cells

Under a previous Thin Film Partnership project a Cu_XTe-based contact deposited by sputtering yielded devices with state-of-the-art performance[1]. Although, no systematic stability study has been carried out on cells contacted with Cu_XTe, during the first year of this project a small number of such cells were included as part of the light soaking experiments. Figure 34 below shows the initial and final (1000 hours) light J-V for two devices fabricated with Cu_XTe of two different thicknesses (left 60Å; right 70Å); these cells were light soaked with the cells discussed in the previous section. The initial performance of the device with 70 Å Cu_XTe suggests that a barrier is present at the back contact (slight "bend over" in the J-V), which increases after 1000 hours of light soaking. However, the I-V of the device with 60Å Cu_XTe does not exhibit any "bend over" before or after light soaking. This is interesting in that, the most common type of degradation mechanism observed in CdTe cells fabricated with Cu-based contacts is associated with degradation/changes taking place at the back contact leading to J-V behavior similar to that observed for the 70Å Cu_XTe. These results suggest that under certain conditions the back contact can maintain its "ohmic" characteristics. Nevertheless, both devices degraded as indicated in table 10, with the device dominated by the back contact barrier exhibiting a larger decrease in both its V_{OC} and FF. The key difference is that the degradation of the 70Å device is dominated by the back contact while the other is associated with changes in the main junction properties. Under a previous project it was suggested that some of the observed changes in devices stressed at different temperatures were related to the main junction and not the back contact [1]. The results on the Cu_XTe samples presented here confirm the fact that the junction can degrade while the back contact remains essentially unchanged. It is certainly possible that

[†] The same behavior described in table 9, was verified for a second device.

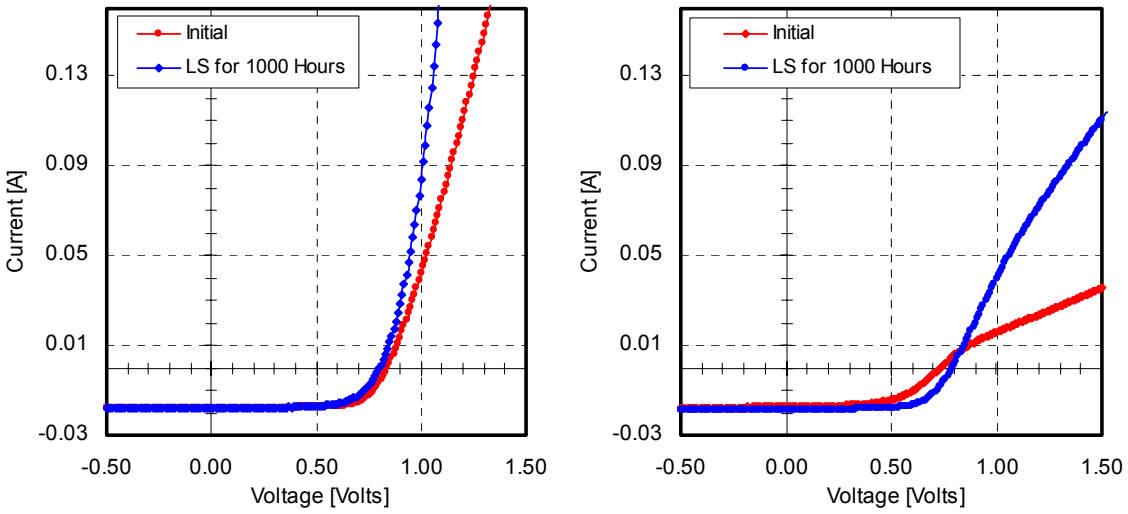


Figure 34. Light I-V for as-deposited and light-soaked for 1000 hours cells contacted with Cu_XTe-based back contacts; left -60Å; right - 60Å

further stressing of these devices will eventually lead to a degradation of the back contact of the device with 60Å of Cu_XTe but this speculation will have to be confirmed.

Table 10. V_{OC} and FF of Cu_XTe-contacted cells before and after light soaking

Sample #	Initial V_{OC} [mV]	V_{OC} after 1000 hours [mV]	Initial FF	FF after 1000 hours
416A4c -	791	740	0.68	0.56
517B3d	840	810	0.72	0.67

7.0 STABILITY STUDIES DATA SECTION

Figure 7.1. Light and Dark J-V for CdTe Cells $CdCl_2$ Heat-treated @ 360°C - Light Soaked @ Open-circuit

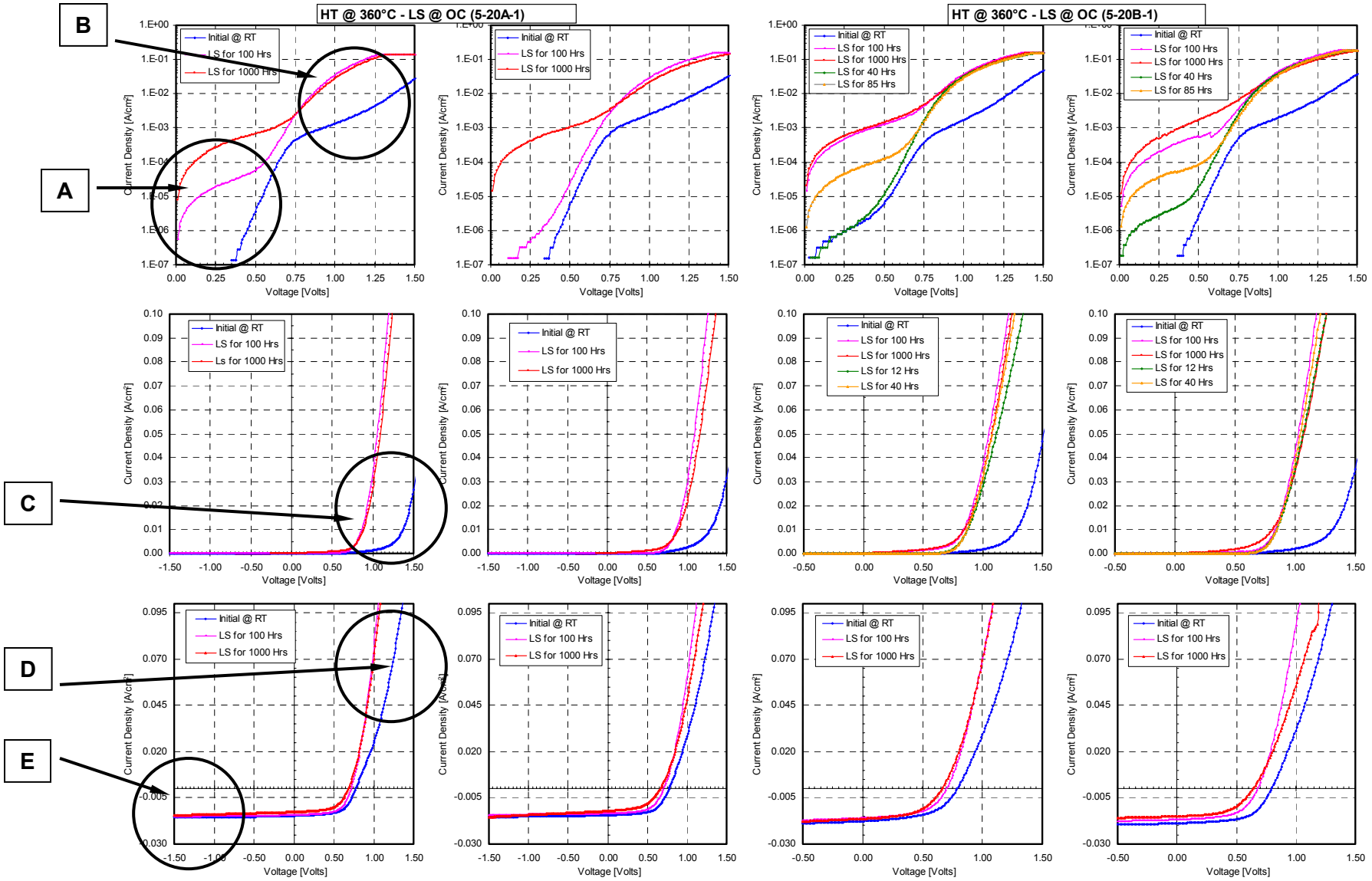


Figure 7.2 Light and Dark J-V for CdTe Cells $CdCl_2$ Heat-treated @ 360°C - Light Soaked @ Short-circuit

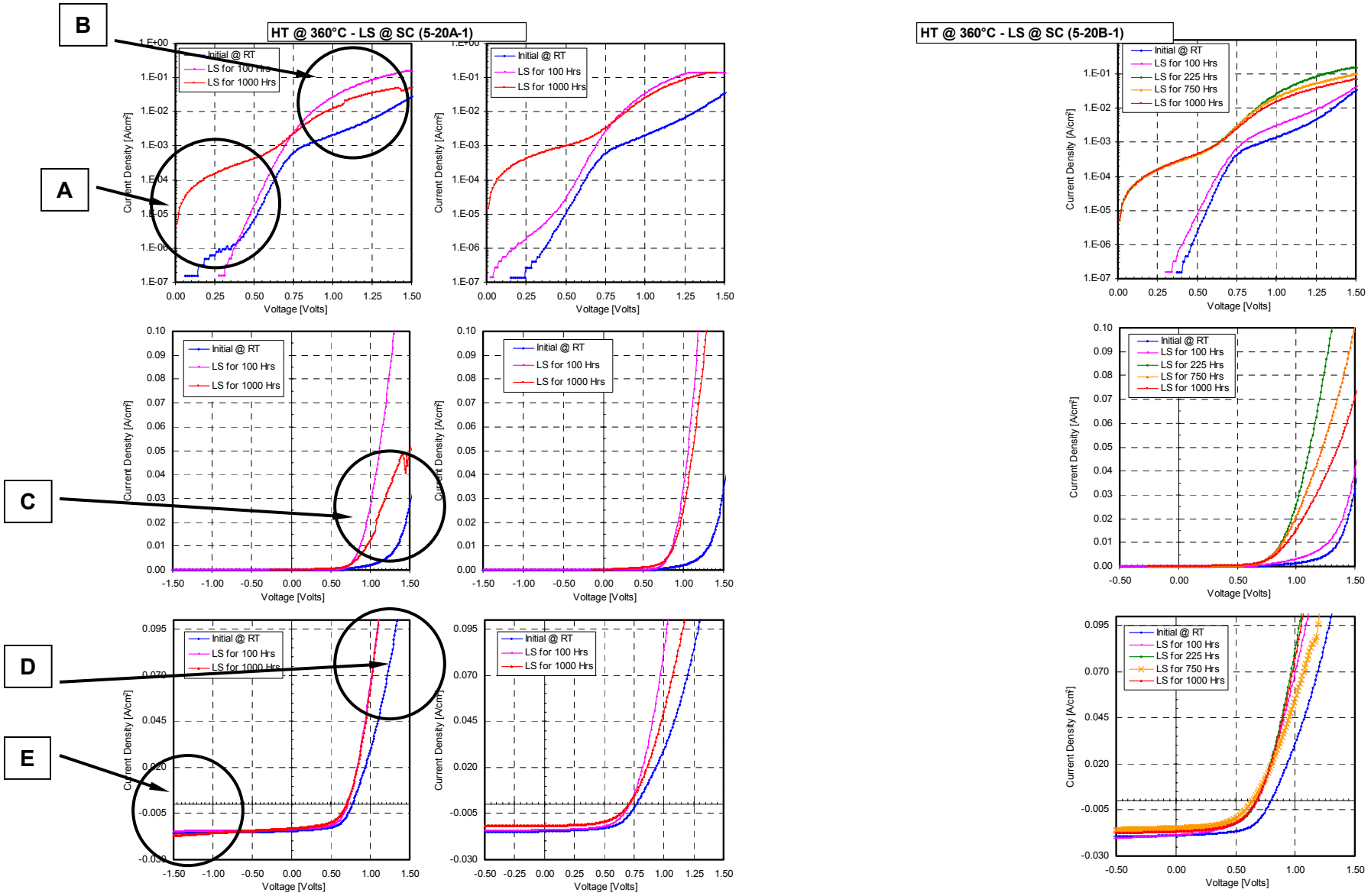


Figure 7.3 Light and Dark J-V for CdTe Cells $CdCl_2$ Heat-treated @ 400°C - Light Soaked @ Open-circuit

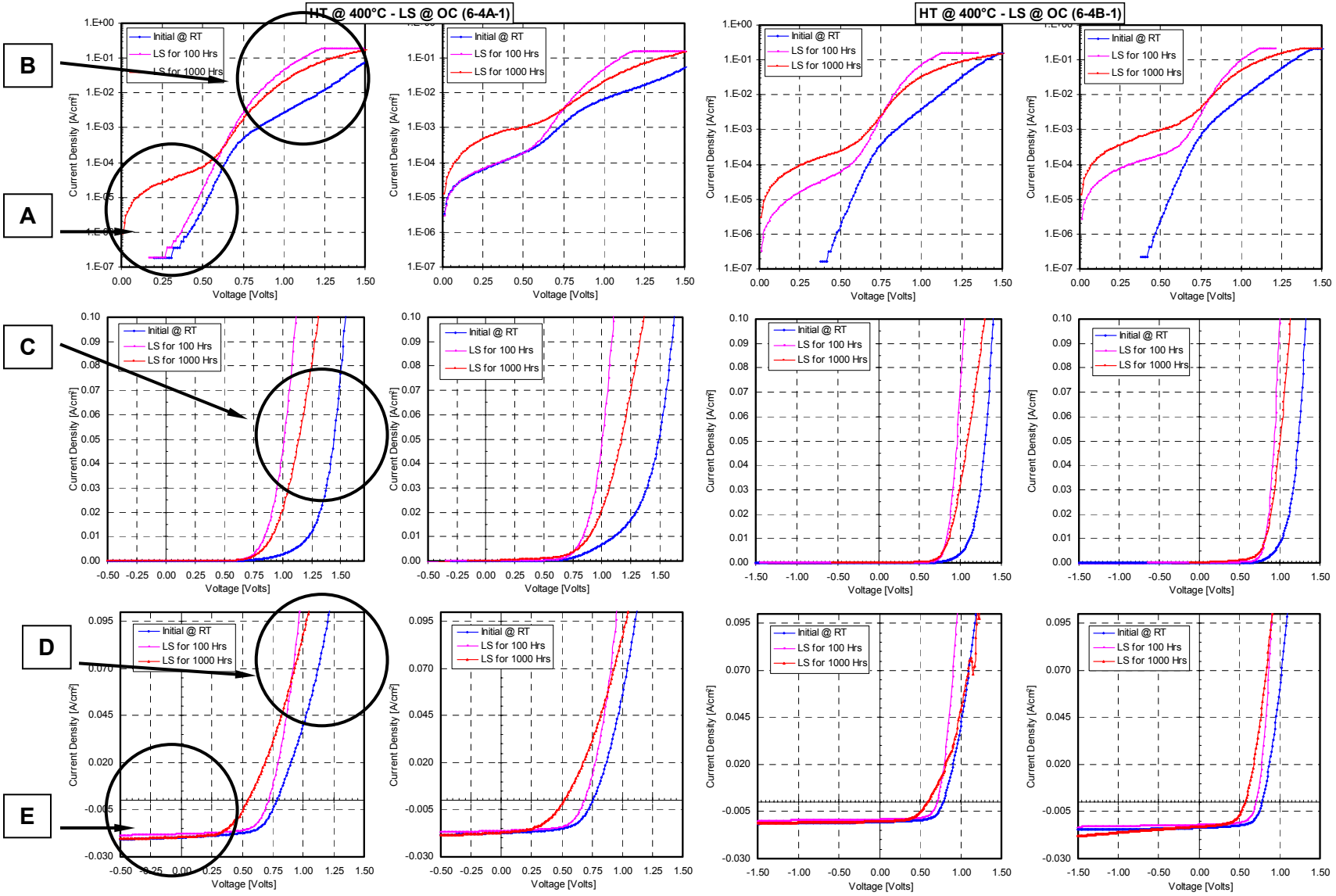


Figure 7.4 Light and Dark J-V for CdTe Cells $CdCl_2$ Heat-treated @ 400°C - Light Soaked @ Short-circuit

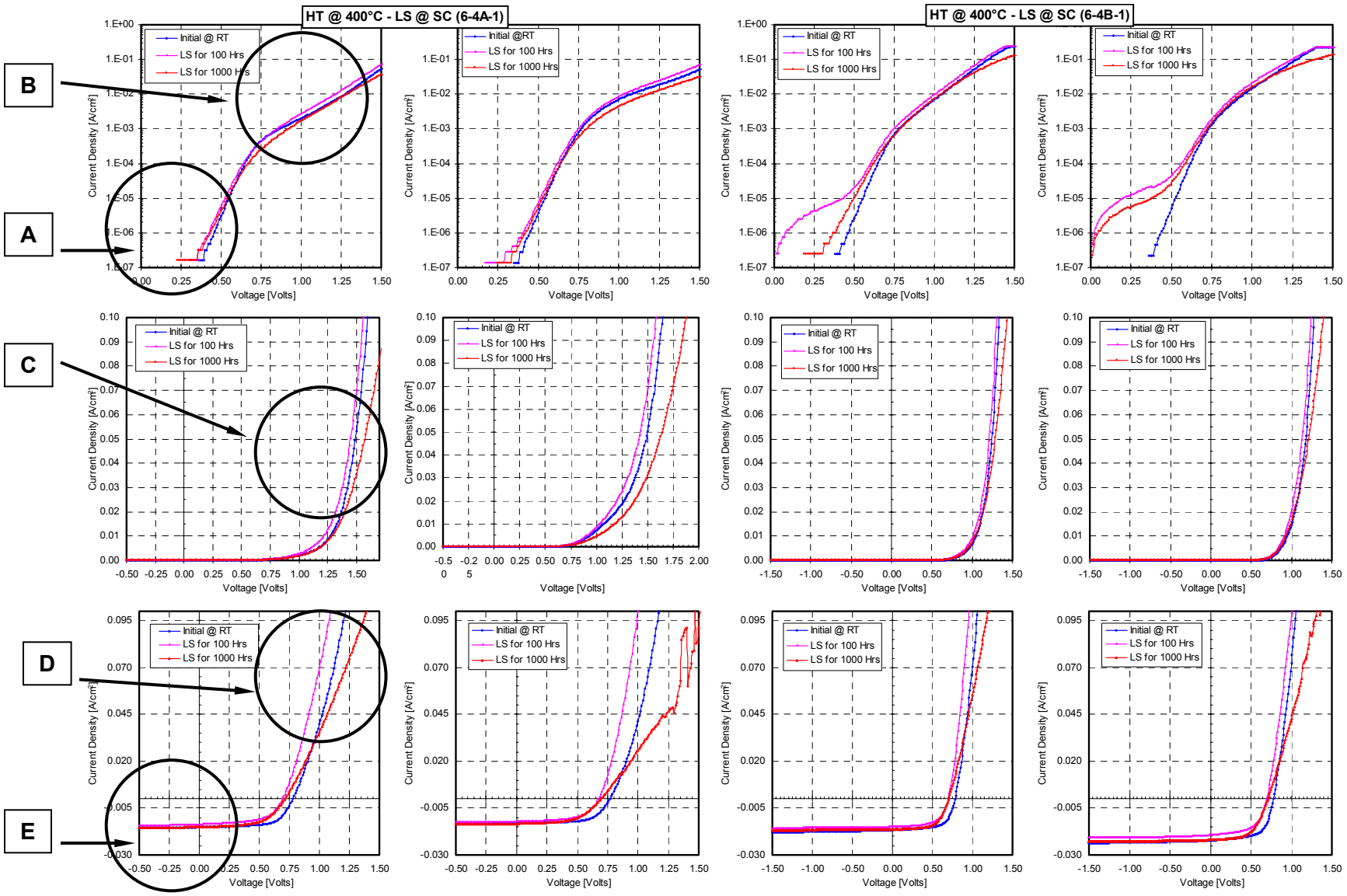
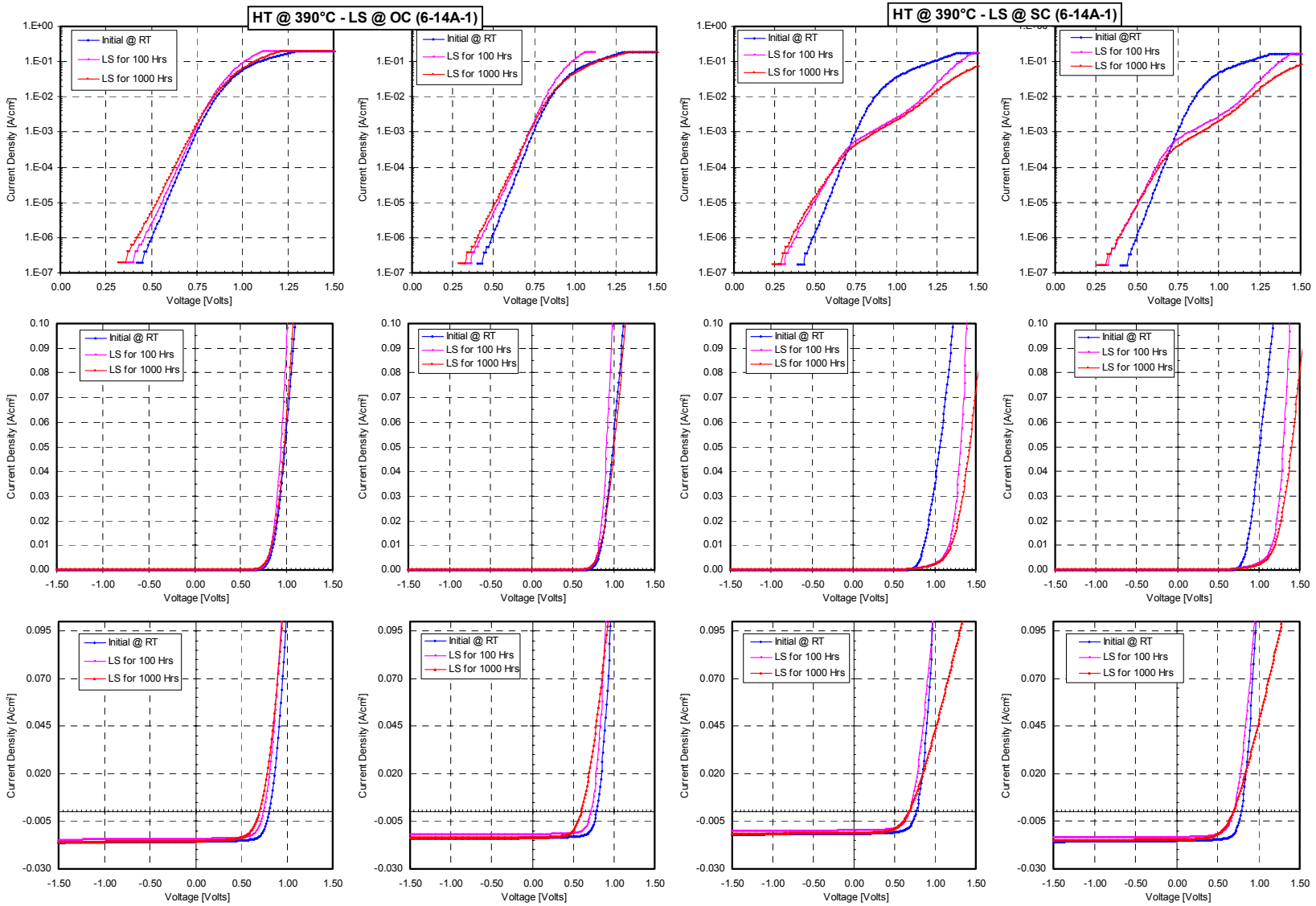


Figure 7.5 **Light and Dark J-V for CdTe Cells $CdCl_2$ Heat-treated @ 390°C Light Soaked @ Open-circuit LEFT and @ Short-circuit RIGHT**



PART II – CIGS

EXECUTIVE SUMMARY

Continuation of development of our manufacturing-friendly 2-step process for CIGS has been accelerated by experimentation with our new in-line prototype processing system. In transferring our baseline process to the new chamber we gained valuable insights that have generic as well as specific implications to our process approach. Two of the primary objectives that drove system design were elimination of selenium flux during metal layer deposition, and better control over water vapor. Both of these objectives have been realized and are leading to significant improvements in process control and understanding. As expected, we have observed an increase in Voc by eliminating background selenium during metal layer depositions. The increase is 20 – 30 mV in our lowest band gap(0.95 eV) devices. Also, control of residual water vapor through use of a load lock has revealed a substantial dependence of both Jsc and Voc on the ambient conditions in the chamber. Voc swings of 75 mV and Jsc swings of 5 mA are commonly observed. This is a confounding variable in our old chamber that in many cases dominates over the intended variables in a set of experiments. This has required the need for large data sets to properly test an idea. Understanding and control over this variable in the new chamber is now expediting experimentation.

With this added control over the processing environment we are gaining valuable insights to film growth mechanisms. Our best devices have had band gaps in the 0.98 – 1.02 eV range. To our surprise we have not been able to make devices with band gaps above 0.95 eV with our baseline process in the new system. We have determined that this is due to elimination of selenium flux during metal layer deposition. It appears that in order to open the band gap it is necessary to have Cu_xSe_y present in the precursor. By eliminating the background selenium flux during Cu deposition we eliminated this species and raised Voc, but in doing so pinned our band gap at the 0.95 eV level. In further studies of this behavior we have also gained new insights to Ga incorporation. By varying from our baseline process we are able to open the band gap, but there appears to be a quantum shift that occurs from the 0.95 eV level up to the 1.1 eV level. We had some evidence of this in the old chamber, but it is much more apparent in the new system because of the increased control. These insights are providing opportunities for improving performance, but are also defining the limitations to performance imposed by the 2-step process. As a result, a set of processing rules is emerging.

Efforts continue to develop alternative buffer layers. To improve understanding of the underlying mechanisms and hopefully find a suitable replacement for CdS we have worked with ZnO and ZIS, and now have added ZnSe. There is increasing evidence that zinc compounds may succeed, and ZnSe is an obvious choice to consider. We are finding that the properties of ZnSe can vary over a large range depending upon the deposition conditions. We have had good success with it as a contact on CdSe and are attempting to transfer this to CIGS. Initial CIGS devices are suffering from low Jsc's, though show promise.

Ongoing efforts continue to model and simulate device performance to help guide our fabrication efforts. Our current device model is based upon defect assignments from the NREL Theory Group. Much of our current effort is focused on the role of the barrier layer. Recent results indicate that band offsets play a dominant role and largely determine the affect of other variables. In particular we find that our low band gap devices are at a disadvantage compared to 1.1 eV devices in terms of finding alternative buffer layers. These insights are driving our processing approach back toward larger band gaps.

1.0 INTRODUCTION

This project is a continuation of efforts to develop an all-solid-state, 2-step manufacturing process for CIGS solar cells. Given the prolonged commercialization efforts based upon the current leading technologies it is apparent that improvements in the manufacturing approach are desired, if not needed. Details of our deposition process have been described previously [1]. We provide a brief description here for convenience. Our substrate is soda lime glass, which we purchase from the local hardware store. A standard glass cleaning procedure is used, and the glass substrate is heated in vacuum prior to Mo deposition by sputtering. Varying combinations of metal or metal selenide layers are deposited by sputtering or evaporation. These precursor layers are then annealed in a selenium flux through a temperature profile with a maximum temperature of 550 ºC. Several process recipes are presently under development, and each involves specific precursor layers and anneal profiles. Much of what is presented in the following discussion is for our baseline process. In this process the order of deposition of the precursors is Cu/Ga/(In + Se). Deviations from this procedure will be presented as they arise in the ensuing discussion. Formation of the semiconductor layer takes about one-half hour. The substrate is finally turned into a device using standard procedures for CBD CdS followed by high ρ/ low ρ ZnO. In our original system the sources were located to give rise to compositional gradients to enrich the data base. To get as much mileage as possible out of a run we fabricate 5 x 5 arrays of 0.1 cm^2 devices by using a shadow mask for the ZnO deposition. The arrangement of sources around the substrate is shown in Fig. 1.

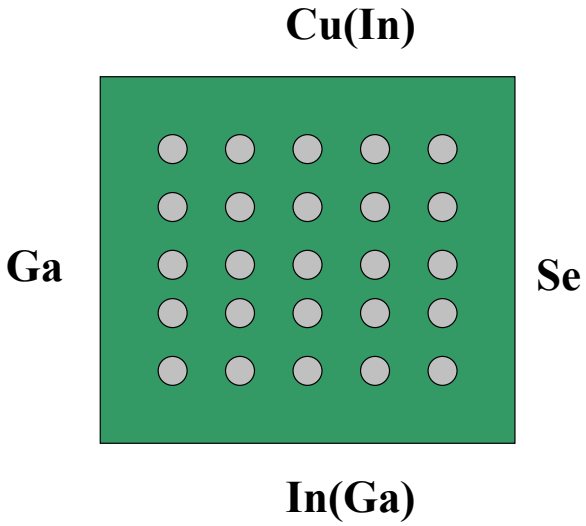


Figure 1. Arrangement of sources around the 2" x 2" substrate for the original chamber. For the new chamber Cu and Se are uniform, and the sides of highest In and Ga composition are shown in parentheses

During the course of our earlier investigations we determined that our processing system had limitations that were limiting the reach of our experiments. For our primary baseline process we deposit free standing layers of Cu followed by Ga. Since Se is also deposited in the chamber, Se is everywhere, and during these metal depositions it is clear that some Se flux is hitting the substrate. We expect that this is contaminating the metal layers and affecting subsequent film formation. To overcome this limitation we designed and built a new in-line system with a load lock. A schematic is shown in Fig. 2. The two main objectives of the design were to control atmospheric contamination effects and to eliminate Se from the metal layers. The results of having attained these will be discussed below. Also, the new system largely eliminates the intentional gradients of the original system. Cu and Se are fairly uniform, although, as will be discussed below, gradients in the Group III elements are still operative. The location of maximum content for the Group III elements in the new system are shown in parentheses in Fig. 1. Additional details will be provided in the discussion that follows.

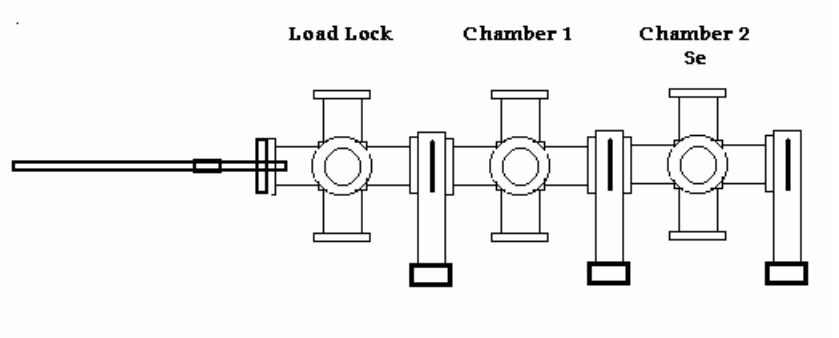


Figure 2. Schematic of our new in-line chamber

The results provided below consist of three main topic areas. The first and major thrust area is progress made using the new deposition system. A particular issue that we address is transfer of our process recipe from the old system to the new system. This is always a challenge and typically leads to new insights that partially quell the expected frustrations. The second topic is progress with alternative buffer layers, and the third is modeling and simulation, primarily focused on buffer layers. The latter two topics are those related to TFP group activities with the junction sub-team.

2.0 CIGS PROGRESS – NEW DEPOSITION SYSTEM RESULTS

2.1 Initial Observations

Although we have good control over short circuit currents with our baseline process in our original system, Voc's and FF's exhibit large fluctuations. This forced the need to conduct a large number of runs so that suitable statistics would be available to determine the outcome of a specific experiment. While we made some progress in this mode, it was slow, and as performance improved, it became increasingly difficult to verify the outcome of new ideas. Runs in the new system indicate a significant improvement in this situation. Voc's and FF's are consistent. We are confident that the changes that we make in a run are what causes changes in performance. While the exercises that we are conducting are specific to our process, there is generic content to what we learn that can be useful to other processing approaches.

Our first concern was to transfer our baseline process from our original system(system 1) to the new system(system 2). As expected, device performance was different, though poorer. Since we can run the same process side-by-side in the two reactors, the different performance in the new system makes it clear that performance is sensitive to the uncontrolled background parameters in system 1, and most likely specifically to the background Se flux. We had been convinced of this previously by noting differences in performance as we took measures to reduce the background flux in system 1. But we were never able to eliminate the flux completely, and we had no way of knowing how sensitive the process was. Having now eliminated the flux completely we are observing several effects. Firstly, we had some difficulty with adhesion and had to lower the Ga level from 600 Å to 400 Å. This solved the problem and produced reasonable devices with reproducible performance. By direct comparison with devices from system 1 we determined an increase in Voc of 20 – 30 mV. This is what we were expecting, though more. And, unfortunately this was accompanied by a drop in Jsc. This was surprising in that we had always been able to maintain high Jsc's in system 1. QE spectra indicate that the loss is due to a sloping spectral response, that is, low red response. We have

associated such behavior with the presence of poorly bonded Ga through numerous studies in the past and suspect that this is the case here.

Our original hypothesis from past observations is that depositing Cu in the presence of a Se flux was producing a Cu_xSe_y species some fraction of which was surviving subsequent processing. The remnants of this species was diminishing Voc. The modest increase of 20-30 mV realized thus far suggests that we have reduced or eliminated this loss by eliminating the Se flux during Cu deposition. However, in the process we have lost control over other loss mechanisms. First, the adhesion issue suggests that depositing Ga in the presence of Se flux helps tie up the Ga so that it does not interfere with adhesion. And, the presence of Se flux during Cu and Ga deposition apparently gives rise to better Ga bonding. Therefore what we are making at this point in the new system benefits from reduction of the Cu_xSe_y species but suffers now from less effective Ga bonding and adhesion to the substrate.

In attempting to understand the current loss at a microscopic level we have used the defect model of the NREL theory group[11] as input to the AMPS© simulation code. Device performance is best explained in terms of acceptors and acceptor defects. (Further discussion of this will be provided below. Here we just excerpt a result that is appropriate to discussion of Jsc loss.) In particular we have found the Cu vacancy defect to correlate best with observed behavior. In Fig. 3 we show the effect of this defect on QE response. The n and i layers correspond to the surface and bulk regions of the device. As this defect is increased in either region there is loss in Jsc that spectrally is a good match to our experimental results. We can not easily justify why this defect would increase due to poor Ga bonding at this time. We can only speculate that Ga deposited in the presence of Se is more able to allow Cu to bond with it and In_xSe_y to form CIGS. A reduction in the number of Ga_xSe_y species doesn't let Cu into the lattice as readily resulting in more copper vacancies.

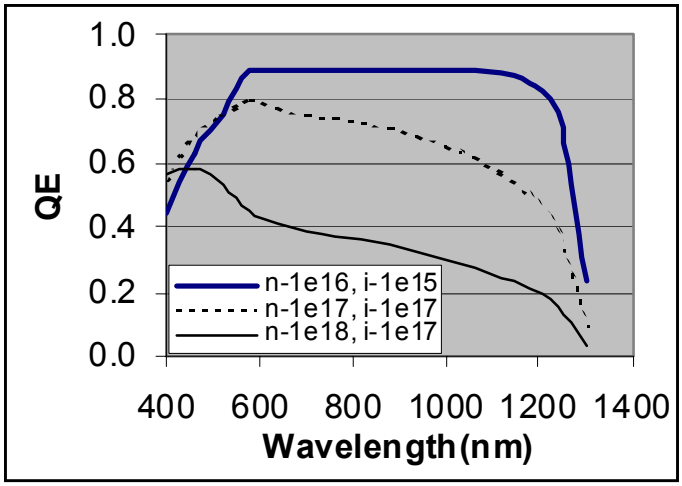


Figure 3. QE response as a function of the V_{Cu} level in the i and n CIGS layers indicated in the legend

Through ongoing experimentation we have gained additional insights to the mechanisms affecting Jsc. These are the result of differences in procedures between a load-locked and non-load-locked system. In system 1 the bell jar was opened between runs to remove and reload substrates. And on an irregular basis source materials were replenished and maintenance performed. This resulted in varying exposure time of the inside of the chamber to ambient conditions. Since the system is equipped with a fast pump, however, and the run was started after reaching a baseline pressure(~2 x 10^{-7}), pump down time before deposition did not vary much. In retrospect this likely resulted in a run-to-run variable background of water vapor. The process recipe that we developed in this chamber neutralized this variable in that we had good run-to-run reproducibility for Jsc. However, since system 2 is load-locked, it is not surprising that the process recipe does not transfer directly. What we have determined is that in system 2 Jsc is a function of the history of exposure to ambient, that is, how long the chamber was exposed, and how many runs have been completed since opening the chamber. Thus Jsc's are low on

the first run after exposure and improve with subsequent runs thereafter. The Jsc and QE response for two run sequences are shown in Figs 4 and 5. As can be seen, the biggest increase is between runs 1 and 2. And for sequence 2 some bouncing occurs after run 1. The QE responses indicate both upward shifts and red-favored increases. The mechanisms giving rise to this behavior are under study.

This behavior is an interesting contrast with the constancy of Jsc in system 1. This suggests (putting aside differences in Se flux for the moment) that if water vapor is always present at about the same level, a process recipe can be found to accommodate that scenario. However, if water vapor is present for the first run and then diminishes with subsequent runs, the run process has to be tuned accordingly. It should be possible to pump longer before the first run to bring the water vapor within acceptable limits before the first run. This should result in a fixed process recipe. If this takes too long, it would then be necessary to adjust conditions from run to run to account for the changing water vapor level.

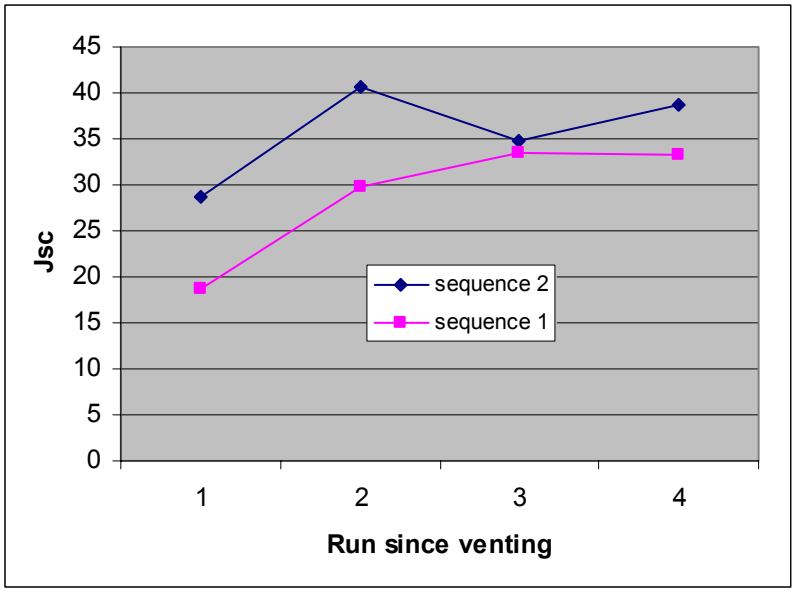


Figure 4. Jsc dependence on run number following chamber venting for two sequences

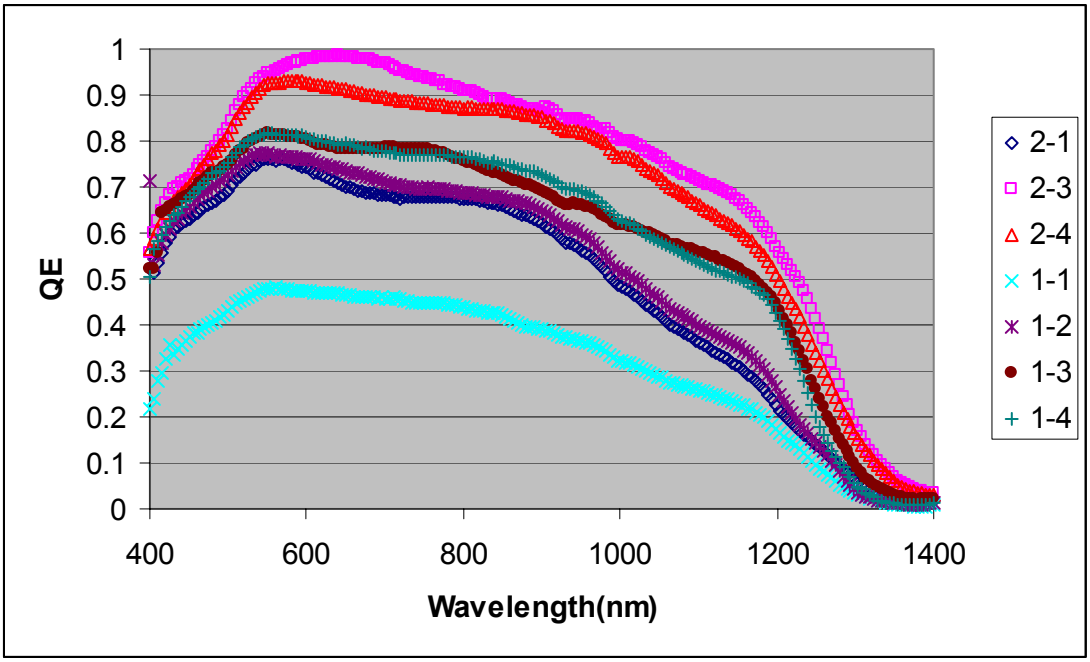


Figure 5. QE response as a function of run number following chamber venting for two sequences

Another question that this raises is why is the first run in system 2 not good when it has about the same water vapor level as system 1, and the same process recipe is being run? There are several possible answers, and we are conducting experiments to sort this out. First, the pumping in system 2 is not nearly as fast as that in system 1, so after exposing system 2, it may take a lot more pumping time relative to system 1 to get the water vapor level down. To ferret this out we have conducted several experiments in which the run conditions were varied. A primary design and operating principle was to not allow selenium in chamber 1 in which the Cu/Ga precursor layers are deposited. Another difference that is turning out to be important is the pumping configuration. The original system has a large diffusion pump and cold trap. The in-line system has a turbo pump and cold trap on chamber 2, but only a turbo pump on chamber 1.

We first address the concerns that we had expressed regarding deposition of the Cu/Ga precursor layer in the presence of background Se. An obvious question is whether the Ga layer, the Cu layer or both are adversely affected by the presence of Se. To sort this out we deposited the Cu layer in chamber 2 that should have a background flux similar to that in the single chamber. We then transferred the substrate to chamber 1 to deposit Ga in the selenium-free environment. Following Ga deposition the substrate would then follow the standard procedure of transfer to chamber 2 for In/Se deposition and selenization in Se flux. The initial results from this sequence were a bit confusing, and it was only after several runs that we noticed an interesting pattern emerging. A major new occurrence was the occasional production of devices with band gaps in the 1.1 eV range. Using our standard process for the in-line system we have not seen band gaps above 0.95 eV, so the up-shift in Eg is clearly attributable to the new process sequence. However, the shift is not consistent. It seemingly comes and goes from run to run. Voc's are jumping around as well. We suspected that this again has to do with the environment inside the chamber and proceeded to test the effect of those conditions.

To sort this out we vented one or the other of the chambers or both before runs and then tracked behavior in subsequent runs. The results of a run sequence are shown in Fig. 6. Prior to run 12 both chambers (c1 and c2) were vented. As indicated, the device peeled from the substrate. In run 13 Voc was 320 mV and in 14 and 15 up to 440 mV. Prior to run 16 c1 and c2 were vented again, and Voc dropped down to the 380 mV range. Before run 18 only c2 was vented. There was already some evidence that Voc was climbing, and in run 19 it was up to 450. C2 was again vented before run 20 and Voc dropped slightly to 430 mV. It is apparent that the primary cause of the Voc swings is venting chamber 1. A smaller effect may be attributable to chamber 2. The bottom line is that Voc is down by about 70 mV following venting. These swings in Voc are accompanied by band gap shifts as well. Since this was not observed previously, it is clear that the combination of depositing Cu in chamber 2(notably in the presence of Se) and the condition of the chambers relative to venting are dramatically affecting the band gap and Voc's. The results attained thus far support an explanation based upon the formation of Cu_xSe_y species in

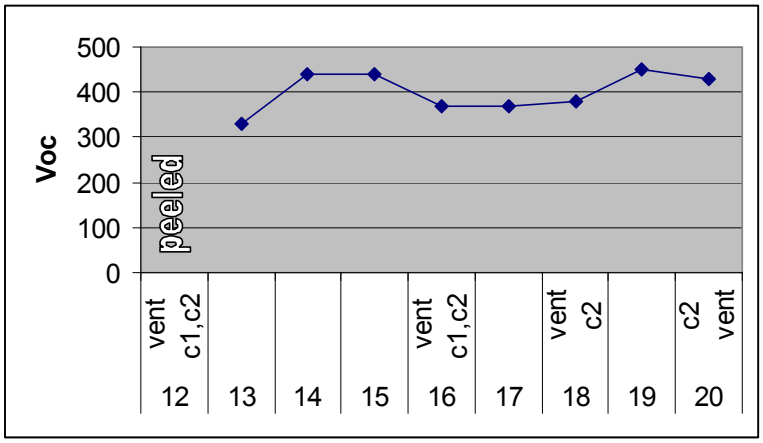


Figure 6. Dependence of Voc on run sequence following venting in the in-line system

chamber 2, and the discussion that follows is based accordingly.

2.2 Band Gap Shift

One of the interesting observations that we have made in the new system is an unexpected effect of system environment on band gap. One of our original motivating factors for going to a two-chamber design was to eliminate exposure of the precursor metals to Se during their deposition. We had evidence from our single chamber results indicating that Se contamination from background flux was limiting Voc values. In the new system design we only deposit metals in chamber 1 and take precautions to keep Se from chamber 2 from back diffusing into chamber 1. For example, when we open the gate valve between the chambers, we make sure that we are pumping from chamber 2 so that the driving vacuum force is from chamber 1 toward chamber 2. However, the consequence of eliminating Se from the metal precursors is surprising. Using the same baseline process from the original system in the new system we are not able to affect an increase in band gap above the 0.95 eV level that is basically the CIS band gap. As we raise the Ga level while lowering the In level performance diminishes dramatically to the point where the QE spectrum is no longer viable. This behavior is in stark contrast to that obtained when we deposit Cu in chamber 2. Because of the presence of the Se source in chamber 2 there is a background flux of Se during Cu deposition just as in our old system. Following Cu deposition in chamber 2 we transfer the substrate back to chamber 1 for Ga deposition and continue with the standard run sequence. In this case, however, we are able to open the band gap. This indicates that band gap increases are associated with a Cu_xSe_y species being present in the precursor. It would seem that Ga can only enter the lattice successfully if this is the case. Further discussion of the consequences of this result will follow, but data associated with this observation will be provided first.

In Fig. 7 we show QE spectra for runs with Cu deposited alternately in the two chambers. Run 288 is a standard run with Cu deposited in chamber 1. It also has 200 Å of Ga deposited in chamber 1. As can be seen, while there is a sharp downturn in the response at 1100 nm, there is tailing out to 1300 nm and beyond. The band gap is ill defined in this case, but the response out to 1300 nm and beyond indicates the presence of a low band gap contribution. Run 289 is the same as 288 except that it has a 300 Å Ga layer. As can be seen, rather than opening the band gap this produces a response that is more clearly dominated by a low band gap component below 1.0 eV. Actually the poor response of run 288 is in part due to a high Cu/Group III metal ratio. We do this intentionally because this is the best way to get Ga into the lattice, and our best devices have been those for which this ratio is close to unity. Thus the improvement in QE response is largely due to a reduction in Cu/Group III due to the addition Ga, however, the additional Ga is not resulting in an increase in band gap. It is commonly known that Ga and In segregate to the back and front of the cell respectively[12], and thus it can be understood that the additional Ga is not entering the space charge layer. If it were,

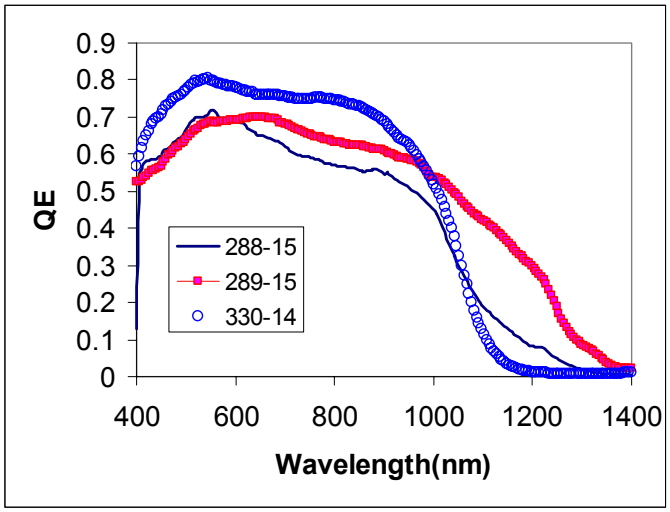


Figure 7. QE response of CIGS films for which Cu was deposited in chamber 2(288,289) and in chamber 1(330). Runs 288 and 330 had 200 Å of Ga, and run 289 had 300 Å of Ga.

and if it were properly bonding in that region, there would be an indication in the QE spectrum. Adding more Ga results in deterioration of device performance because it is unable to bond properly into the lattice.

In run 330 the Cu is deposited in chamber 2. It also has 200 Å of Ga deposited in chamber1. As can be seen, the QE spectrum indicates a "clean" band gap of about 1.1 eV. Ga is clearly entering the lattice in the space charge region giving rise to this obvious shift. Since the only difference is the deposition of Cu in chamber 2 in the presence of background Se flux, we must conclude that this is responsible for the band gap opening.

Additional insights to this mechanism are provided by examining Fig. 8 which shows QE spectra for three individual devices from this run. Since the substrate was stationary during these depositions, there are gradients in the composition across the sample. In this case the gradients of interest are the Cu/In and Cu/Group III ratios that are increasing from sample 11 through 12 to 14. As can be seen, at low ratios(device 11) evidence of a low band gap component is evident. At device 12 with somewhat higher ratios the long wavelength tail is diminished, and finally at device 14 with still higher ratios the tail is all but gone. Thus to have Ga successfully bond in the space charge region three conditions appear to be necessary:

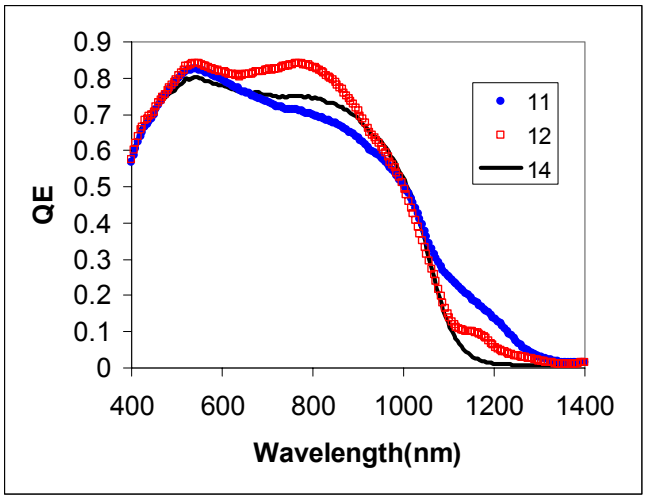


Figure 8. QE spectra of devices from run 330 in which Cu is deposited in chamber 2. Cu/In and Cu/Group III are increasing from device 11 to device 14.

1. A Cu_xSe_y species must be present.
2. Cu/In must be above 1.
3. Cu/Group III must be near 1.

The first condition is a necessary precursor for Ga to bond in the space charge region. The second condition is necessary for Ga to compete with In for lattice sites. Only if there are missing In sites in the space charge region will Ga successfully bond there. The third condition indicates that if excess Ga is added beyond that which can bond successfully, some is likely to end up in the space charge layer as defects hurting device performance. This is seen in Fig. 8 by comparing the spectra for devices 12 and 14. In the wavelength region below 1000 nm the spectrum for device 12 is higher than that of 14. Device 14 shows a downward sloping response in this region due, we expect, to excess Ga.

Evidence of the low band gap residual in devices with a nominal band gap of 1.1 eV raises the questions of where this residual layer is located and what effect it has on performance. Since it is clearly in the space charge region, it may be expected to cause a reduction in the effective band gap which would limit Voc. In Fig. 9 we show the dependence of Voc on the QE at 1200 nm for a series of four runs. Our test structures consist of an array of 25 devices on the 2" X 2" substrate (Refer to Fig. 1). Several representative data points from each run are plotted. A linear fit through the data would indicate virtually no dependence. However, there are reasons to suspect that this is not the case, and the second order polynomial fit showing a peak in the

center is likely closer to the truth. A plot of the same data for the individual devices is shown in Fig. 10. In this case linear fits for two of the devices are included and indicate opposite trends. One might expect the absorption tail as represented by QE at 1200 nm to be indicative of inferior material, in which case there should be a monotonic increase in Voc with decreasing QE at 1200. Run H319 clearly shows this trend over its range, but run H315 shows the opposite trend. This suggests competing mechanisms with the two runs on opposite sides.

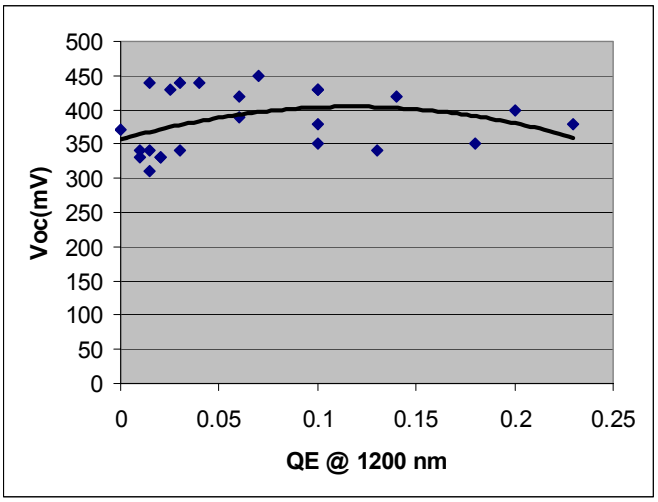


Figure 9. Dependence of Voc on QE at 1200 nm for a series of runs

To examine this issue more closely we focus on the details within a single run. As indicated above we have a rich data set of a matrix of 5 x 5 devices across the substrate. Although we have made an effort to reduce compositional gradients in this system they still exist to some extent. Cu and Se are fairly uniform across the substrate. However, In and Ga gradients are about 12% and 29% respectively in the top to bottom direction at this point. These can be further reduced, but for now are left large intentionally to enrich the data base while sorting out these mechanisms. These gradients are in fact responsible for the behavior seen in Figs 9 and 10. In Fig. 11 we show the profile of Voc for a run in which Cu is deposited in chamber 2 to open the band gap, and the Cu/Group III ratio is high. (This is run 330 re Fig. 8 above.) The "In" and "Ga" labels indicate the side of highest composition for each metal respectively, and they each drop off toward the other direction with the gradients indicated above. Thus in going from column 1 to column 5 the deposited In level is decreasing by 12%, while Ga is increasing by 29%.

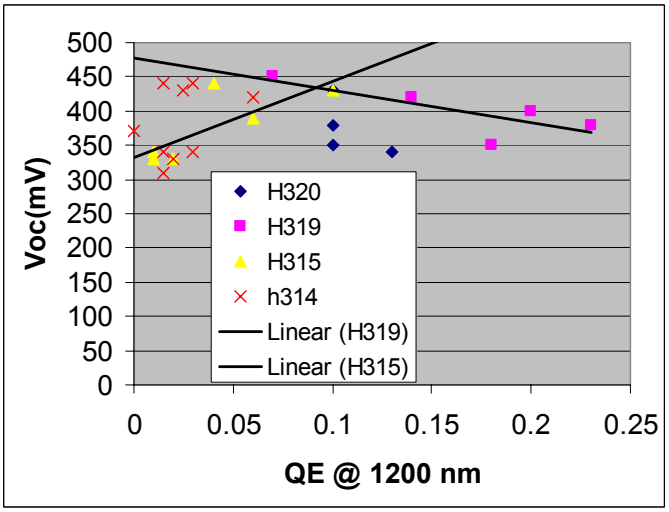


Figure 10. Dependence of Voc on QE at 1200 nm for the devices of figure 9

As can be seen, there is a monotonic increase in Voc from columns 1 to 3, but beyond that there is obvious drop off and spottiness in the Voc values. The overall behavior is seen more clearly in Fig. 12. Here we show both Voc and FF behavior for the average of the 5 devices on each row with the same In and Ga composition. Since Cu and Se are fairly uniform, the behavior is mainly due to interplay between In and Ga. As we go from column 1 to column 3 there is opening of the band gap and reduction of the long wavelength tail as discussed above. This is a regime of "favorable" Ga incorporation, and our interpretation is as follows. In the space charge region for the composition of column 1 Cu/In $\geq$ 1, and a small amount of Ga is allowed to enter the lattice. As we proceed toward column 3, as In drops off, more Ga enters the lattice, still in a somewhat favorable manner, since Voc is increasing. However, at this point the band gap is about 1.1 eV and Voc should be above 600 mV. As we allow more Ga and less In

to enter the lattice the Voc peaks and then heads down. Beyond column 3 replacing In with Ga is resulting in significant deterioration of performance including complete shorting in some cases. While Voc at first benefits from the addition of Ga due to band gap opening, FF deteriorates across the whole range. This is a strong signal that adding sufficient Ga to raise the band gap is deteriorating the electronic properties. This is not unlike similar observations that we made with the old system in the past. However, we now have more insights to the mechanisms that lead to this behavior. Two things in particular come to mind. First we know that the presence of a Cu_xSe_y species in the precursor is what is allowing Ga to enter the lattice. The second is that there is a quantum shift in band gap in going from our base 0.95 eV material to material with significant Ga incorporation. The band gap does not shift systematically from 0.95 to 1.1 eV. In fact we are not able to produce material with band gaps within this range. We have made similar observations previously, but did not have sufficient control over processing to nail it down as we have here. A possible source of this behavior is the Cu_xSe_y species in the precursor. It may be that the amount of this that forms determines the level of Ga bonding and thus the band gap. Experiments are planned to examine this possibility.

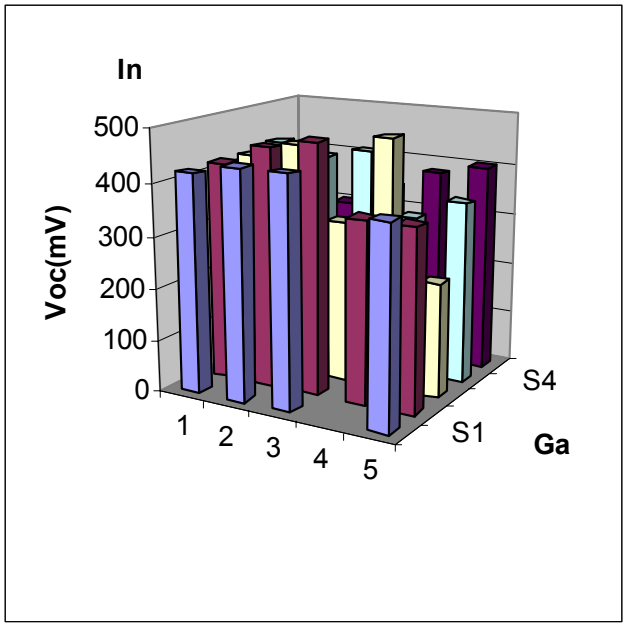


Figure 11. Voc profile for a 5 x 5 array of devices for which the Cu/Group III ratio is high

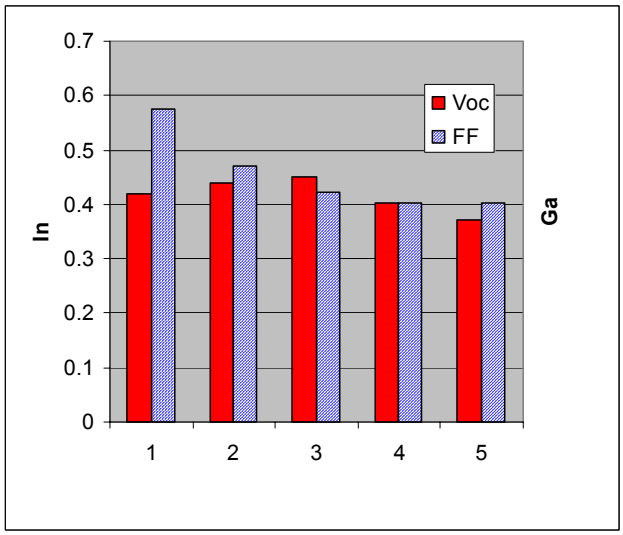


Figure 12. Average Voc and FF along the In to Ga gradient for the data of figure 11

Combining these results with the QE observations above the following emerges. Our material seems to consist of two phases. A 0.95 eV phase and a 1.1 eV phase. Both can be present in the space charge region. We can eliminate the 0.95 eV phase by providing Cu_xSe_y species in the precursor and going to high Cu/Group III ratios. What we don't yet understand is why the 1.1 eV phase is preferred and why the electronic properties deteriorate as this phase is formed. The band gap for optimum performance of co-evaporated material is in the 1.1 eV range, so there is nothing inherently wrong with this composition. In fact it is likely the composition that we need to improve performance, but thus far our path to making it gives rise to additional harmful species. We have several ideas in mind to help us determine the loss mechanisms and eliminate them. For example, we have found that the residual low band gap layer can be eliminated at a lower Ga incorporation level by an extended anneal time at the end of deposition. This might signal more effective incorporation of

Ga resulting in a lower level of harmful Ga species. Experiments are underway to verify the expected improvement in electronic properties. Our focus over the next period will be to better understand these mechanisms and to develop ways of controlling them.

3.0 ALTERNATIVE BUFFER LAYERS

3.1 Modeling and Simulation

We have an ongoing effort to develop alternate buffer layers for CIGS. The ideal would be a Cd-free buffer deposited by some type of physical vapor deposition. Materials that we have studied that meet these requirements include ZnO, In_2Se_3, ZIS and more recently ZnSe. While these efforts are predominately experimental, we also endeavor to improve our understanding of the operable mechanisms to aid in development of junction formation. AMPS© simulations have been used to assist our efforts, and recently we combined it with defect insights from the NREL theory group to upgrade our base CIGS model. The basic device configuration is shown in Fig. 13. Total device thickness is 2.1 μm. Key features of the model are judicious use of the V_{Cu} and (M_{Cu} + 2 V_{Cu}) complex defect pair in the bulk and near surface regions of the device. We are able to attain consistent fit to experimental data for our devices and derive useful insights to overall device performance. A complete discussion can be found in Quarterly Report 5 of the predecessor contract to this, subcontract ZAF-8-17619-29. Using this as our base model we then explored issues particular to buffer layer contacts. Since most of our efforts have been with ZnO buffer layers, we addressed it first to try to resolve some of the experimental observations that we have made over time. Of particular concern is the inconsistent behavior of ZnO as a buffer layer contact, in our own data as well as that of others.

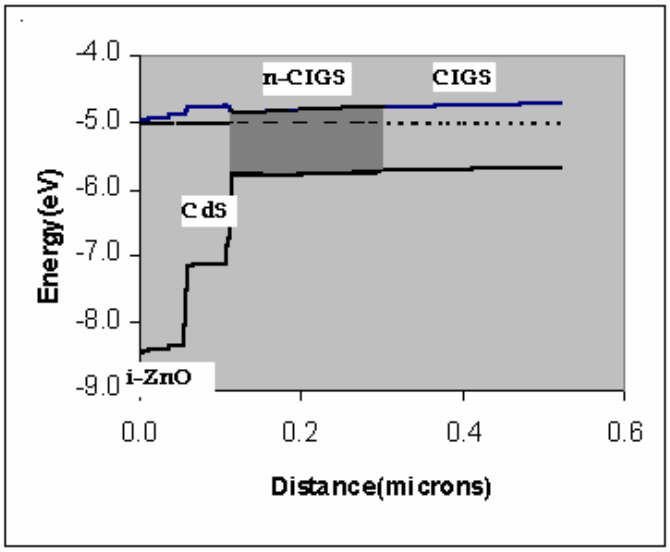


Figure 13. Basic CIGS device configuration in the junction region for AMPS simulation

Our approach was to systematically change key parameters to determine their influence on performance and ultimately to match this with experimental observations. The procedure for ZnO is summarized in table 1. The “Reference” at the top is the best fit to our highest output baseline cells. “Standards” at the bottom provides some of the key parameters for the various layers. What we are specifically addressing here is the effect of increasing the thickness of the ZnO layer. In the first entry we double the ZnO thickness in the standard cell, and there is no change. In the next entry we remove the CdS layer and performance improves. This, however, does not account for passivation effects that CdS may provide at the interfaces. It only addresses the bulk properties of the layers. Next we lower the electron affinity to 3.8 from 4.0 and start to see an effect on the FF as the ZnO thickness is increased. This becomes even more evident below as the affinity is lowered to 3.6 in a structure with CdS present again. Finally as we lower the mobilities in the ZnO layer we see additional loss of FF and losses in Jsc. The device is now very sensitive to the ZnO thickness which is consistent with experimental observations. In Fig. 14 we show IV curves for some of these configurations relative to the

Experiment	Eff	Jsc	Voc	FF	Observation
Reference	13.5	37.8	0.49	0.68	
Add 55 nm ZnO	13.5	37.8	0.49	0.68	unchanged
Remove CdS	14.1	38.6	0.49	0.71	Should be slightly better
ZnO affinity - 3.8	14.1	39.4	0.48	0.71	
Add 55 nm ZnO(affinity of both - 4.0)	13.9	36.7	0.49	0.72	
ZnO affinity of both - 3.8	9.3	37.6	0.48	0.48	FF collapse: consistent with experiment
Reference					
ZnO affinity - 3.8, thickness - 110	13.3	37.3	0.49	0.69	little effect
ZnO affinity - 3.6	13.6	38.2	0.48	0.7	
ZnO affinity - 3.6, thickness - 110	11.3	36.4	0.48	0.6	FF drop, some Jsc drop
ZnO affinity - 3.6, mobilities -0.1	7.2	36.8	0.48	0.38	FF collapse, some Jsc drop
ZnO affinity - 3.8, mobilities -0.1, thickness - 110	10.6	36.2	0.49	0.56	FF collapse, some Jsc drop
Standards					
CIGS band Gap	0.95				
CIGS affinity	4				
CdS affinity	3.9				
CdS thickness	55				
ZnO affinity	4				
ZnO thickness	55				
ZnO mobilities	10				

Table 1. AMPS simulation results for ZnO buffer layers.

reference cell. The collapsing FF and losses in Jsc are consistent with experimental observations. An important insight that this provides is the sensitivity to electron affinity. What is important here, in fact, is conduction band offset. As this becomes larger as the affinity of ZnO is decreased, many of these phenomena start to kick in. We are particularly sensitive to this issue because our baseline devices have a band gap of 0.95 eV. This is a 150 mV offset disadvantage relative to typical high efficiency devices with band gaps of 1.1 eV. This indicates that our devices are particularly sensitive to ZnO properties and explains some of the fluctuations that we have observed. This kind of insight is important to choices we make in terms of ultimate device design. Based upon these results we are in fact now spending more

effort on development of devices with a 1.1 eV band gap. The challenge of Ga incorporation becomes more difficult as discussed above, but we avoid needing to find a replacement for ZnO.

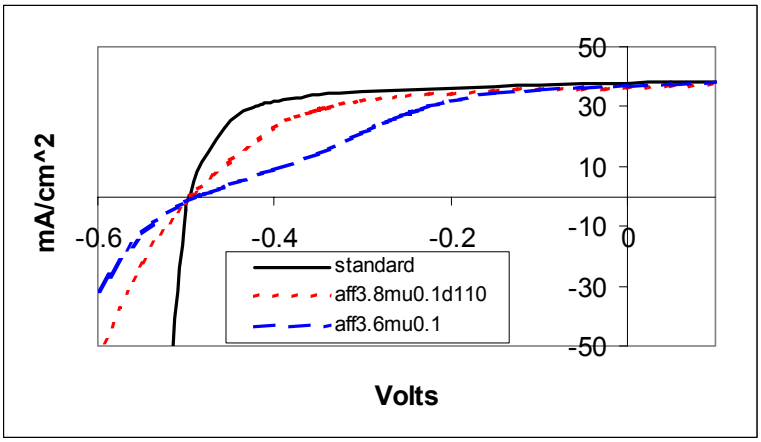


Figure 14. AMPS IV curves for a ZnO/CdS/CIGS device with various ZnO properties

3.2 ZnSe

Another buffer layer that we and others have had under investigation is Zinc Indium Selenide(ZIS). With either ZnO or ZIS replacing CdS we have attained performance comparable to, but just a notch below, that of baseline CdS devices. A natural follow-on to this work is ZnSe. It has about the same electron affinity as ZnO but a lower, though acceptable, band gap(2.6 eV). Of interest is the difference in chemistry at the interface. Replacing oxygen with Se results in one less element at the interface, since Se is of course already present in the CIGS. ZnSe is also under consideration as a window layer for our CdSe and CZT devices that are sponsored under the High Performance Project, so this project benefits from those developments. A major difference, however, is that the Hiper project requires p-type ZnSe, while here the buffer layer need not have a particular type, but should not be strongly p-type. Understanding and controlling these contact layers is important to both projects, and thus both benefit from study of materials of mutual interest.

For our purposes here the first priority is to develop high electronic quality, undoped ZnSe. The meaning of “high electronic quality” turns out to be a variable here. That is, our best CdSe devices are made with ZnSe deposited onto a room temperature substrate in a chamber with a background Se flux. Though this material is apparently of low density and may have a high Se vacancy level, it nevertheless works well as a contact to CdSe. In terms of our needs here this material seems inferior. We find that deposition at substrate temperatures in the 200 – 250 ºC range and in the presence of a Se flux produces higher density material that works better as a buffer layer in CIGS devices than the room temperature material.

For these devices the ZnSe is deposited in the CIGS chamber, although there is a vacuum break following CIGS deposition. The usual two-layer ZnO deposition then follows in a separate chamber. A variety of Se flux profiles and substrate temperatures were tried. Unfortunately to date none of the variations that we have tried has resulted in good performance. Although this is disappointing, it is nevertheless useful to understand why performance is poorer than the

other zinc-based buffer layer options. In Fig. 15 we show IV curves that are typical of the results attained thus far. In this case there was no Se flux and the layer was deposited to a thickness of 200 Å at room temperature. As can be seen, all parameters are low. The primary telltale, however, is the slope under reverse bias. This indicates a significant carrier collection loss problem. Our early thoughts on this are that the ZnSe layer is too resistive and is causing parasitic voltage loss. The QE plot for a companion device is shown in Fig. 16. The integrated Jsc is 11.6 mA/cm2, and as can be seen, the profile is square, but the entire curve has been shifted down nearly a factor of four relative to a typical CdS device. In fact, if the proper Jsc of 40 mA/cm2 were being generated, based upon the dark IV curve Voc would exceed 400 mV as expected. This offers some hope. The dark IV is reasonably proper, so the overall performance shortfall is related to carrier collection.

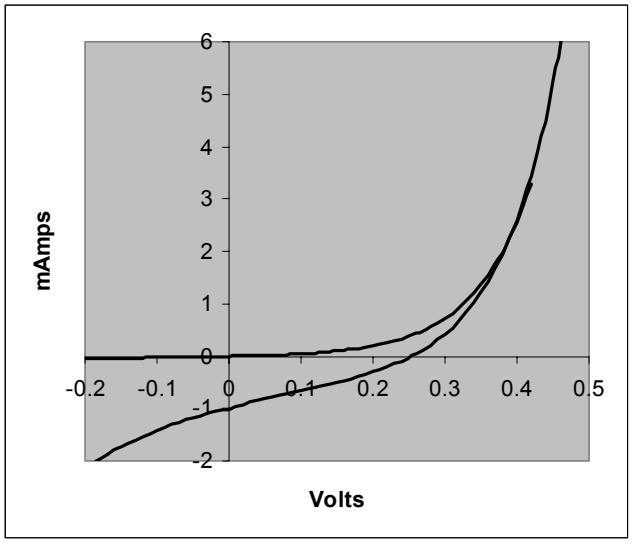


Figure 15. Typical IV curve for ZnSe/CIGS devices

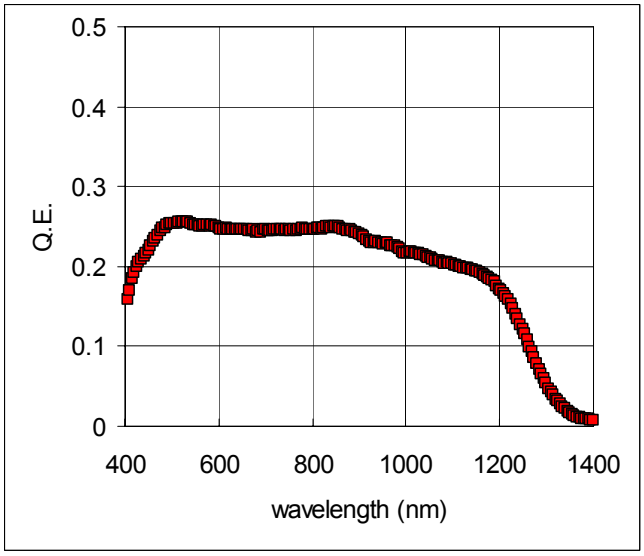


Figure 16. QE spectrum for a ZnSe/CIGS device

We have observed such behavior previously with the undoped ZnO layer in standard CdS buffer layer devices. In Fig. 17 we show IV data for standard ZnO(doped)/ZnO(undoped)/CdS/CIGS devices as a function of the undoped ZnO layer thickness. (This can be compared with the AMPS simulations in Fig. 14.) The stretching out of the IV curve as the thickness increases is evident, and gives rise to a large slope under reverse bias similar to that above for ZnSe buffer layer devices. However, unlike ZnO the IV curve for ZnSe above does not exhibit substantial crossover. We observe some crossover in other ZnSe devices, but it is substantially less than that for ZnO. As discussed above, we have been simulating the behavior

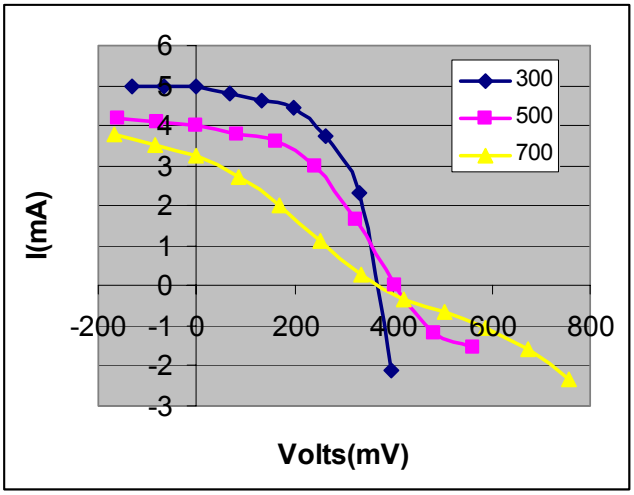


Figure 17. IV for CIGS devices with varying undoped ZnO layer thickness

exhibited by the various buffer layer options with AMPS and are gaining insights to the underlying mechanisms. Crossover, for example seems to arise from a combination of factors rather than a single one. Further details will be provided in upcoming reports. Meanwhile we will continue efforts to relax the parasitic voltage behavior of the ZnSe layers that we have deposited thus far. If this can be achieved, we expect significant improvement in performance.

NATIONAL TEAM ACTIVITIES

The University of South Florida continues to actively participate in the CdTe and CIGS National Teams. Contributions during the last CdTe team meeting Oct 28, '02, are listed below:

CdTe

1. Provided eight substrates with varying CdTe thickness for experiments to take place at First Solar (First Solar Focus Group activity).
2. Fabricated solar cells using CdTe plates provided by BP Solar for as part of the $CdCl_2$ heat treatment activity.
3. Carried out J-V-T measurements and provided data to Dr. Fahrenbruch for modeling activities planned for the meeting
4. Carried out C-V characterization for USF samples, and samples provided by CSU for comparative studies.

CIGS

USF has undertaken activities in support of the junction subgroup of the TFP team.

- Simulation and modeling of junction mechanisms using AMPS© and the defect models from the NREL Theory Group.
- Fabrication and evaluation of devices with alternative buffer layers including ZnO, ZIS, In_2Se_3 and ZnSe.

These are discussed in the main text and were the topics of two presentations given at the last TFP meeting in Denver.

Acknowledgements

AMPS© is a copyrighted device simulation code developed by Penn State University under sponsorship of the Electric Power Research Institute.

REFERENCES

1. "Advanced Processing of CdTe- and $CuIn_{1-X}Ga_XSe_2$- based Solar Cells", Annual Reports 1,2 & 3, Subcontract # ZAF-8-17619-29, submitted to NREL.
2. Wu. X, R. Ribelin, R. G. Dhere, D. S. Albin, T. A. Gessert, S. Asher, D. HG. Levi, A. Mason, H. R. Moutinho, and P. Sheldon, "High Efficiency $Cd_2SnO_4/Zn_2SnO_4/Zn_XCd_{1-X}S$/CdS/CdTe Polycrystalline Solar Cells", *Proceedings of the 28th IEEE Photovoltaic Specialists Conference*, Anchorage, (2000), pp. 470-474.
3. Wu X., P. Sheldon, T. J. Coutts, D. H. Rose, and H. R. Moutinho, "Application of Cd_2SnO_4 Transparent Conducting Oxides in CDS/CdTe Thin Film Devices", *Proceedings of the 26th IEEE Photovoltaic Specialists Conference*, Anaheim, (1997), pp. 347-350.
4. T. J. Coutts, D. L. Young, X. Li, W. P. Mulligan, and X. Wu, "Review Article: Search for improved transparent conducting oxides: A fundamental investigation of CdO, Cd_2SnO_4, and Zn_2SnO_4", Journal of Vacuum Science and Technology A18, 6 (2000) 2646.
5. X. Wu, W. P. Mulligan, and T. J. Coutts, "Recent Developments in RF Sputtered cadmium stannate", Thin Solid Films 286 (1996) 286.
6. R. Mamazza, U. Balasubramanian, D. L. Morel, and C. S. Ferekides, "Thin Solid Films of $CdIn_2O_4$ as Transparent Conducting Oxides", *Proceedings of the 28th IEEE Photovoltaic Specialists Conference*, New Orleans, (2002), pp. 616-619.
7. Wu X., S. Asher, D. H. Levi, D. E. King, Y, Yan, T. A. Gessert, and P. Sheldon, J. Applied Physics,, 89, 8, (2001) pp. 4564-4569.
8. Wu. X, R. Ribelin, R. G. Dhere, D. S. Albin, T. A. Gessert, S. Asher, D. HG. Levi, A. Mason, H. R. Moutinho, and P. Sheldon, "High Efficiency $Cd_2SnO_4/Zn_2SnO_4/Zn_XCd_{1-X}S$/CdS/CdTe Polycrystalline Solar Cells", Proceedings of the 28th IEEE Photovoltaic Specialists Conference, Anchorage, (2000), pp. 470-474
9. B. E. McCandless, H. Hichri, G. Hanket, and R. W. Birkmire, "Vapor Phase Treatment of CdTe/CdS Thin Films with $CdCl_2$:O_2", Proc. 25th IEEE PVSC, 1996, pp.781-7842
10. N. Romeo, A.Bosio, R. Tedeschi, Solar Energy Materials & Solar Cells, Vol 58, 1999, pp. 209-218.
11. Su-Huai Wei, S. B. Zhang, and Alex Zunger, Appl. Phys. Lett., 72(4), 3199 (1998).
12. K. Lindahl, D. Olson, J. Moore, A. Schwartzlander, R. Noufi, "Quantitative Investigation of Reactions in Copper-Indium-Gallium Multilayer Thin Films", Proceedings of the 25th IEEE Photovoltaic Specialists Conference, Washington D. C., May, 1996, p 949.